

FPGA Implementation of Hybrid Test Data Compression Method Using Scan Chain Compaction and Dictionary-based Scheme

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Abstract- The Goal in this paper is proposal of new test data compression method for reducing test data volume and test application time. The existing system in this paper is group the scan chain in the ascending order and it must be in odd number for group and the number of element in the groups. The proposed method consists of two steps: scan chain compaction (even or odd) and dictionary-based compression scheme. The scan chain compaction provides a minimum scan chain depth by using compaction of the compatible scan cells in the scan chain. The focus is to compacted scan chain is partitioned to the multiple internal scan chains it may be odd or even for using the fixed-length index dictionary-based compression scheme that provides the high compression ratio and the fast testing time. The proposed compression methods scan chain which is not arranged in ascending order and not in odd number. Hence it produces the output with four groups and it is implemented in FPGA using VHDL coding, where the existing system produces five groups, system delivers compressed patterns from the ATE to the chip and drives a large number of multiple internal scan chains using only a single ATE input and output. Experimental results for the test benches show that the test data volume and testing time for the proposed method are less than previous compression schemes.

Index Terms- test data compression, test application time, full-scan circuit, scan chain compaction, dictionary-based compression scheme

I. INTRODUCTION

As the complexity of very large scale integration (VLSI) circuit increases, testing plays an important role in today's system design. One of the most important factors in driving up the test cost is increasing the amount of test data volume, which is a result of the large size of the designs and the new types of defects appearing in the advanced manufacturing process. A large amount of test data must be stored in the automatic test equipment (ATE) and transferred deep into the chip as fast as Possible. Since the channel capacity and the size of memory of ATE are limited, the test application time and the test power have been significantly increased. The test data compression technique offers a promising solution to the problem of increased the test data volume for SOC testing.

Several test data compression schemes have been proposed for reducing test data volumes. These previous schemes of compression techniques can be categorized into two groups:

code-based schemes and structural schemes. In the code-based schemes, a number of techniques based on FDR coding, VIHC coding, RF-Huffman coding, and Selective-Huffman coding, have been proposed to reduce test data volume. Although these compression methods can achieve high compression ratio, the test application time is not sufficiently reduced, because of the long shifting time to drive into the full-scan chain. Additional synchronization and handshaking between the SOC and the ATE can be occurred in decompression decoder by using multiple clocks to increase testing speed. Several dictionary-based compression methods have been presented to reduce SOC test data volume. To get high compression results, these methods need the memory or large size hardware circuit to store dictionary entries.

In the structural compression method, the Illinois scan architecture use an external input port to drive multiple internal scan chain inputs without any logic gates; it provides the reduction of test data volume and testing time. However, additional fault simulation and test generation are necessary to achieve high fault coverage. Additionally, if the faults are hard to be detected by using the parallel mode of the Illinois scan architecture, the test vector needs to be driven serially into a single long scan chain. The scan chain reconfiguration method has been proposed in the form of an XOR-based. This method identifies the compatibility of scan cells in the scan chain, and then the scan chain network is constructed by XOR gates The scan chain has a shorter scan chain depth than a traditional scan chain. It can provide the reduction of test data volume and test application time simultaneously. However, if the test data cube does not contain enough compatible scan cells, the effect of reducing scan chain depth is restricted.

In this paper, we propose a new effective test data compression method using the scan chain compaction and the dictionary-based compression scheme. The first method, the scan chain compaction constructs a scan chain network which has minimum number of scan slices; the number of scan slices is scan depth, similarly in [11]. The small size of scan chain depth can reduce total data volume and test application time; because it needs less scan chain shifting operation to drive test data bits into the scan chain. However, the reduction of scan chain depth by the compaction is limited, if the test vector does not have enough compatible scan cells.

To achieve high compression ratio, we combine the dictionary-based compression scheme with the scan chain compaction. The scan chain network composed by the scan chain compaction is divided to the multiple internal scan chains to

reduce the scan shifting time using the dictionary-based compression scheme. The decoder of proposed dictionary-based scheme drives the test vector in to the whole multiple internal scan chain inputs at the same time, as it can help to reduce the test data volume and test application time. The hardware overhead can be kept reasonable size because we use the dictionary which has fixed-length indices and the small amount of the index entries which are already compressed by the scan chain compaction. The proposed compression scheme uses the test data vector generated by the traditional ATPG and delivers high compression ratio and fast application test while retaining the original faults coverage without any additional fault simulation and test generation. The proposed compression architecture is implemented with only one single scan-in and scan-out pin externally, although the multiple scan chains are consisted internally. Experimental results for large ISCAS-89 benchmark circuits show that proposed compression method could reduce test data volume and test application time significantly.

II. OVERVIEW OF PROPOSED SCHEME

A. Definitions:

To present the proposed test data compression algorithm simply, several definitions are used

Definition 1. Scan Frame: A scan frame is a vector of inputs applied to the same scan cells in each test pattern,

Which contains the number of 0s, 1s and don't-cares (Xs).

Definition 2. Direct compatible: If scan frames of two scan cells in the scan chain never receive conflicting binary values in totality for the same test cube, these two scan chain are direct compatible, and can be driven the same test data.

Definition 3. Inverse compatible: If scan frames of two scan cells in the scan chain never receive identical binary values in totality for the same test cube, these two scan chain are inverse compatible, and can be driven the same test data by inserting inverter on the scan path.

B. Overall algorithm of the proposed scheme:

The overall framework of our compression scheme for scan based on circuit is shown in Fig. 1. The proposed scheme uses the test data cube of the full-scanned circuit, the test cube is generated by traditional ATPG without any additional fault simulation and test generation. Since the test vectors generated by the ATPG have large number of don't care bits, there are many compatible or inverse compatible scan cells in the full-scanned circuit. All compatible or inverse compatible scan cells are identified

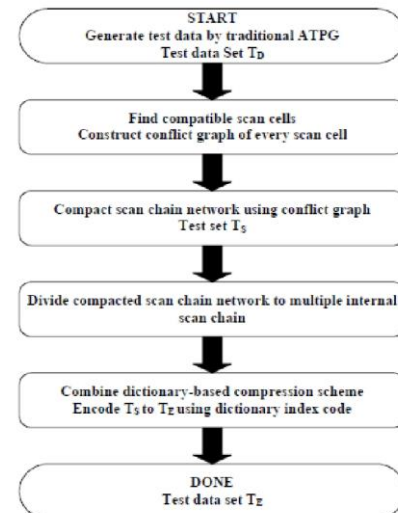


Fig. 1 Overall framework of the proposed scheme

and composed to groups of scan cells which have same test values for all test vectors. To find the maximal number of scan cells in a group, the conflict graph for all scan cells is used. The scan chain can be constructed to the compacted scan chain network using the conflict graph of scan cells. The compacted scan chain network has a shorter scan chain depth than a conventional scan chain. The short scan chain depth can provide the reduction of the test data volume and test application time simultaneously. Although the scan chain is compacted to the scan chain network with short scan depth using the conflict graph, the reduction of scan chain depth is limited when the test vector does not have enough compatible scan cells. To alleviate this limit and achieve high

Compression ratio, the new dictionary-based compression scheme is combined with the scan chain compaction. To use the dictionary-based compression scheme, the compacted scan chain network is divided to the multiple internal scan chains. Each slice vector of the multiple internal scan chains is driven into the all scan chain inputs at the same time. The slice vector has a fixed length and which is a symbol of the dictionary. The symbol is encoded to the fixed length dictionary index that is shorter than the length of the symbol. Therefore the proposed dictionary-based compression is the vertical compression that presents not only the reduction of the test data volume and application time but also the use of only a single ATE channel. The original test vector TD can be compacted and encoded to the significantly compressed test vector TE by combining the scan chain compaction and the dictionary-based compression scheme.

III. SCAN CHAIN COMPACTION

The proposed scan chain compaction methodology aims at constructing a scan network with minimum scan depth. Such a solution perfectly exploits the structural relationship between scan cells to deliver the highest compression ratio while retaining the original faults coverage. There are many scan cells which are direct or inverse compatible with other scan cells in the full scan chain. These scan cells compose the compatible scan cell group,

all scan cells in the same group are always driven identical bits (direct compatible) or never identical bits (inverse compatible). All scan cells in the same group can be injected the same test data value at the same clock cycle. Therefore the compacted scan chain network can be constructed and each compatible scan cell group becomes one depth of the scan chain network.

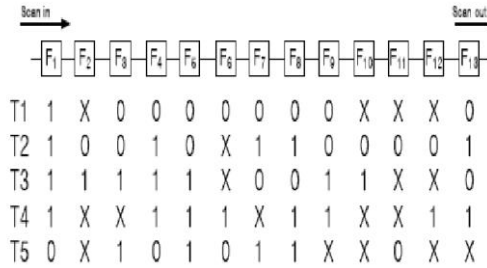


Fig. 2 Sample of single scan chain and test vector

The scan network expands and compacts depending on the compatible scan cell group sizes resulting of varying numbers of scan cells. To construct the scan chain network, the types of expansion and compaction mechanisms within the scan network are defined.

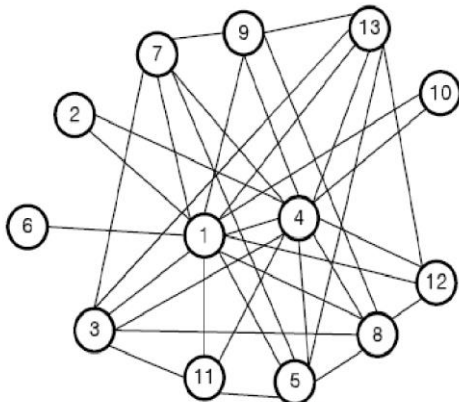
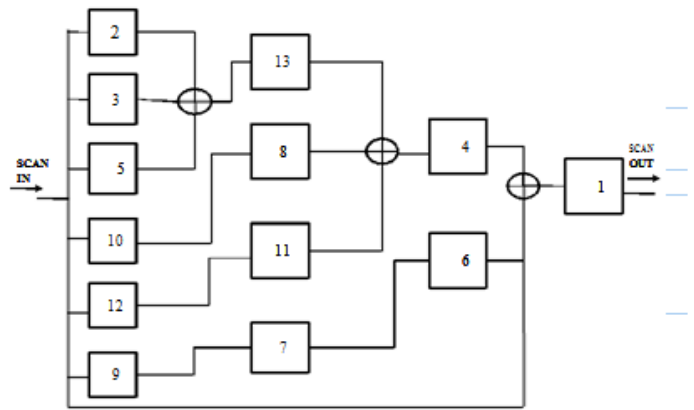


Fig. 3 Conflict graphs for scan cells in Fig 2.

The expansion mechanism in the form of a fan-out network allows in scan cells within the compatible scan cell group to always receive identical bits, although the group sizes may vary. The expansion expands the test data value from a single scan-in pin or small size groups to the large size groups with the fan-out network. The compaction mechanism uses XOR gates to compact the test data value from the larger size group to the next smaller size group. A series of such expansions and compactions construct the compacted scan chain network between a single scan-in and scan-out pin. The number of the compatible scan cell groups between scan-in and scan-out pins constitutes the scan depth, and as many shift cycles will be required for each test vector. We present two rules on group sizes to ensure the delivery of always identical bits to the scan cells within the same group, and avoid certain aliasing problem in the expansion and compaction mechanisms. First, XOR gates with only an odd number of inputs are used to compact a group into the subsequent group to avoid constant value of generation by the

XOR gates. Secondly, the number of outputs of every expanding fan-out should be odd in order to avoid self-aliasing According to these two rules, each compatible scan cell group should consist of an odd number of scan cells. To achieve the highest compression ratio, the number of depth in the scan chain network is minimized, that depends on the number of compatible scan cell groups. The conflict graph is used to construct the most compact scan chain network. The conflict graph represents the relationship between scan cells for all scan cells in the scanned circuit. The vertices of the graph represent each scan cell, an edge between two vertices exists if and only if two scan cells corresponding to the vertices are incompatible that means these two scan cells cannot belong to the same group. Fig. 3 shows the conflict graph for all scan cells of the single scan chain in Fig. 2. As mentioned in Section II, scan-cell compatibility can be the form of direct or inverse compatibility. Although the proposed method so far has concentrated on the direct compatible case, inverse

Compatibility is also equally beneficial. If two inverters are inserted into the scan path, the inverse compatible can still be treated as compatible.



T1	1	0	0	0
T2	1	0	1	1
T3	1	1	1	0
T4	1	1	1	1
T5	0	1	0	1

Fig.5.sample of constructed scan chain network

Then we construct the conflict graph of these scan cells showed in Fig. 3 to find the compatible scan cell groups by the use of matching lines, {F2, F3 F5, F9, F10, F12}, {F7, F8, F11, F13}, {F4, F6}, {F1}. These ordered scan cell groups are stitched via expanding fan-outs and compacting XOR gates, the sample compacted scan chain network produced by the proposed scheme are given in Fig. 5. The compacted scan network in Fig. 5 reduces the depth of scan chain from 13 to 4, then the test data volume is reduced to 20 ($=4*5$) bits. Similarly, the test application time for each test vector is reduced from 13 clock cycles to 4 clock cycles. The area overhead of the compacted scan chain network is 3-input XOR gates that are used for the compaction mechanism.

IV. DICTIONARY-BASED COMPRESSION SCHEME

The compacted scan chain network, which is mentioned in the previous section, reduces the scan depth of the scan chain, and reduces the test cost. However, if the test data cube does not contain enough compatible scan cells, the effect of the Short scan depth is restricted. Then we combine the dictionary-based compression scheme with the compacted scan chain network to achieve the high compression ratio and the fast application time. To address the dictionary-based compression scheme, the compacted scan chain network which has a single scan-in and single scan-out, is partitioned to the multiple scan chains. We divide the scan network to proper number of scan chains, and balance the depth of each scan chain. If the scan chains are unbalanced, additional dummy scan cells are inserted to make that all the scan chains have the same scan depth. The multiple scan chain composed from the compacted scan chain network presents the reduction of the test application time, however the test data volume is unchanged and additional scan inputs and outputs are required. The hardware overhead for the dictionary logic is a weak point of the proposed scheme like other dictionary-based schemes. However, the hardware overhead can be kept reasonable size because we use a small amount of the test data vector which is already compressed by the scan chain compaction and the dictionary has fixed-length indices.

The proposed dictionary-based compression scheme compresses the test data cube of the multiple scan chains in vertically. The decompress decoder of the scheme receives the compressed test data from the ATE, decompresses the compressed test data, and drives the test vector into the all multiple scan chain input at the same time, it can help to reduce the test data volume and test application time. Fig. 6 illustrates the block diagram of the proposed compression scheme dictionary-based test data compression scheme. In the scheme, an ATE scan-in is driven into the m multiple scan chains of the compacted scan network through the dictionary-based decoder.

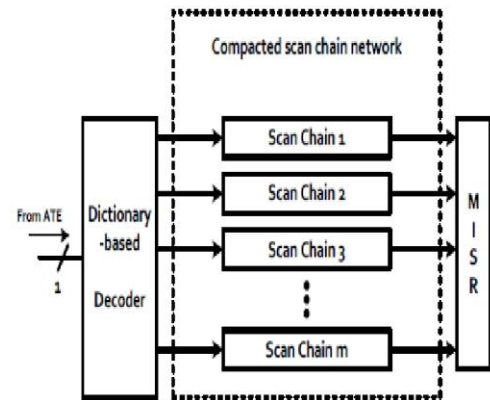


Fig. 6 Illustration of the proposed compression scheme

Each scan slice vector becomes an m-bits symbol, which is encoded to codeword. During the test application, the codeword is shifted into the decoder, after that m-bits symbol is immediately generated by the decoder and driven into the multiple scan chain inputs. The test responses shifted from each scan chain outputs can be compacted by using MISR or other techniques. The proposed decompression architecture assume a 1-to-m scan configuration, in which the number of internal scan chains is m times the number of external scan I/O pins, so significant reductions in the test data volume and test application time can be achieved. The dictionary logic is implemented by using the combination logic circuit. The size of dictionary depends on the length of dictionary index.

Moreover, the proposed dictionary-based compression scheme does not require multiple clock cycles and additional synchronization and handshaking between the CUT and the ATE.

V. CONCLUSION

In this paper, we proposed an effective hybrid test data compression method using the scan chain compaction and the dictionary-based compression scheme. We have shown how proposed test data compression method can be used to reduce the test data volume and test application time for SOC. The Proposed compression method delivers compression patterns from the ATE to the chip and drives a large number of multiple internal scan chains using only a single ATE input and output. The test data volume is compressed twice with the scan chain compaction and the dictionary-based compression, then they can be achieved the highest test data compression ratio and the fastest application time. The proposed compression scheme does not require multiple clock cycles, additional synchronization, and handshaking between the circuit and the ATE. Experimental results for the ISCAS -89 test benches show that the test data volume and testing time for the additional synchronization, and handshaking between the circuit and the ATE. Experimental results for the ISCAS- 89 test benches show that the test data volume and testing time for the proposed

REFERENCES

- [1] R. Chandramouli and S. Pateras, "Testing Systems on a Chip," IEEE Spectrum, pp. 42-47, Nov. 1996.
- [2] A. Chandra and K. Chakrabarty, "Frequency-directed run-length (FDR) codes with application to system-on-a-chip test data compression," Proc. VLSIT est. Symp., pp. 42-47, 2001.
- [3] L. Lei and K. Chakrabarty, "Test data compression using dictionaries with fixed-length indices [SOC testing]," in VLSI Test Symposium, 2003. Proceedings. 21st, 2003, pp. 219-224.
- [4] F.F. Hsu, K. M. Butler and J. H. Patel, "A case study on the implementation of Illinois scan architecture", Proc. Int. Test Conf, pp. 538-547, 2001.
- [5] O. Sinanoglu., "Construction of an adaptive scan network for test time and data volume reduction." IET. Computers & Digital Tech., Vol. 2. no. 1, pp. 12-22, 2008.
- [6] M. Garey, and D.S. Johnson, "Computers and intractability: a guide to the theory of NP-completeness", Freeman, 1979, 1st edn.

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