ISSN 2250-3153

An Overview of Advance Microcontroller Bus Architecture Relate on APB Bridge

Ms. Radhika Koti, Ms. Divya Meshram

Student (M. Tech - VLSI), Priyadarshini College of Engineering, Nagpur - India
Lecturer, Priyadarshini College of Engineering, Nagpur – India

Abstract — The Advanced Microcontroller Bus Architeture (AMBA) is a widely used interconnection standard for System on Chip (SoC) design. An AMBA-based microcontroller typically consists of a high-performance system backbone bus (AMBA AHB or AMBA ASB), able to sustain the external memory bandwidth, on which the CPU, on-chip memory and other Direct Memory Access (DMA) devices reside. This bus provides a high-bandwidth interface between the elements that are involved in the majority of transfers. This paper present three distinct buses and their comparison. By considering merits of APB , AMBA can be design by using HDL.

Index Terms — AMBA, AHB, ASB, APB, Difference of buses

I. INTRODUCTION

Today in the era of modern technology micro-electronics play a very vital role in every aspects of life of an individual, increasing use for micro-electronics equipment increases the demand for manufacturing its components and its availability [4].Embedded system designers have a choice of using a share or point-to-point bus in their designs [2]. Typically, an embedded design will have a general purpose processor, cache, SDRAM, DMA port, and Bridge port to a slower I/O bus, such as the Advanced Micro controller Bus Architecture (AMBA) Advanced Peripheral Bus (APB). In addition, there might be a port to a DSP processor, or hardware accelerator, common with the increased use of video in many applications. As chip-level device geometries become smaller and smaller, more and more functionality can be added without the concomitant [2] increase in power and cost per die as seen in prior generations.

The Advanced Microcontroller Bus Architecture (AMBA) was introduced by ARM Ltd 1996 and is widely used as the on-chip bus in system on chip (SoC) designs. AMBA is a registered trademark of ARM Ltd. The first AMBA buses were Advanced System Bus (ASB) and Advanced Peripheral Bus (APB). In its 2nd version, AMBA 2, ARM added AMBA High-performance Bus (AHB) that is a single clock-edge protocol. In 2003, ARM introduced [2,4] the 3rd generation, AMBA 3, including AXI to reach even higher performance interconnect and the Advanced Trace Bus (ATB) as part of the Core Sight on-chip debug and trace solution.
These protocols are today the de-facto standard for 32-bit embedded processors because they are well documented and can be used without royalties AMBA's target is to help designer of embedded system to meet challenges like design for low power consumption, to facilitate the right-first-time development of Embedded Microcontroller Products with one or more CPUs or signal processors, to be technology-independent and to encourage modular system [4]. To minimize the silicon infrastructure required supporting efficient on-chip and off-chip communication for both operation and manufacturing test [1].

This paper discusses the architecture of AMBA in the section II, section III deals with the various bus methods and their comparison is discuss in section IV. Finally section V and VI gives proposed work and conclude the paper.

II. ARCHITECTURE OF AMBA BASED SIMPLE MICROCONTROLLER

An AMBA-based microcontroller typically consists of a high-performance system backbone bus (AMBA AHB or AMBA ASB), able to sustain the external memory bandwidth, on which the CPU, on-chip memory and other Direct Memory Access (DMA) devices reside. This bus provides a high-bandwidth interface between the elements that are involved in the majority of transfers[3]. Fig1 shows AMBA based Simple Microcontroller. Also located on the high performance bus is a bridge to the lower bandwidth APB, where most of the peripheral devices in the system are located. AMBA APB provides the basic peripheral macro cell communications infrastructure as a secondary bus from the higher bandwidth pipelined main system bus [1]. Such peripherals typically:

(i) Have interfaces which are memory-mapped registers
(ii) Have no high-bandwidth interfaces
(iii) Are accessed under programmed control.

The AMBA specification [2] has become a de-facto standard for the semiconductor industry, it has been adopted by more than 95% of ARM's partners and a number of IP providers. The specification has been successfully implemented in several ASIC designs. Since the AMBA interface is processor and technology independent, it enhances the reusability of peripheral and system components across a wide range of applications.

The AMBA specification [1,3] has been derived to satisfy the following four key requirements.

(i) To facilitate the right-first-time development of Embedded Microcontroller Products with one or more CPUs or signal processors.
(ii) To be technology-independent and ensure that highly reusable peripheral and system macro cells can be migrated across a diverse range of IC processes and be appropriate for full-custom, standard cell and gate array technologies.
(iii) To encourage modular system design to improve processor independence, providing a development road-map for advanced cached CPU cores and the development of peripheral libraries.
(iv)To minimize the silicon infrastructure required supporting efficient on-chip and off-chip communication for both operation and manufacturing test.

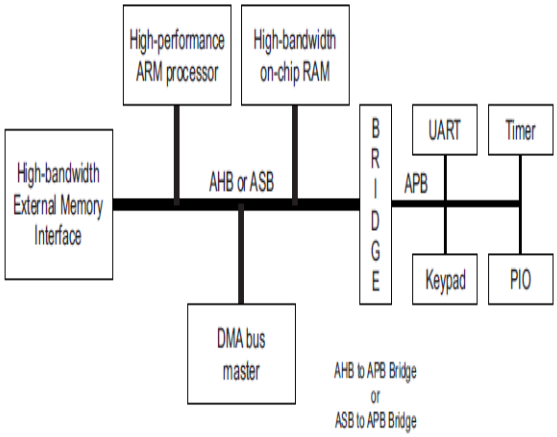

Fig. 1. AMBA based Simple Microcontroller

III. DIFFERENT AMBA BUSES

The Advanced Microcontroller Bus Architecture (AMBA) is ARM's no-cost, open specification[1,3,4], which defines an on-chip communications standard for designing high performance Embedded Microcontrollers. Three distinct buses are defined within the AMBA specification:

(A) The Advanced High-performance Bus (AHB)
(B) The Advanced System Bus (ASB)
(C) The Advanced Peripheral Bus (APB).

(A) The Advanced High-performance Bus (AHB): AHB is a new generation of AMBA bus which is intended to address the requirements of high-performance synthesizable designs. It is a high-performance system bus that supports multiple bus masters and provides high-bandwidth operation. Bridging between this higher level of bus and the current ASB/APB can be done efficiently to ensure that any existing designs can be easily integrated. An AMBA AHB design may contain one or more bus masters, typically a system would contain at least the processor and test interface. However, it would also be common for a Direct Memory Access (DMA) or Digital Signal Processor (DSP) to be included as bus masters.

The external memory interface, APB bridge and any internal memory are the most common AHB slaves. Any other peripheral in the system could also be included as an AHB slave. However, low-bandwidth peripherals typically reside on the APB.

(B) The Advanced System Bus (ASB): ASB is the first generation of AMBA system bus. A typical AMBA ASB system may contain one or more bus masters. For example, at least the processor and test interface. However, it would also be common for a Direct Memory Access (DMA) or Digital Signal Processor (DSP) to be included as bus masters.

The external memory interface, APB bridge and any internal memory are the most common ASB slaves. Any other peripheral in the system could also be included as an ASB slave. However, low-bandwidth peripherals typically reside on the APB.

(C) The Advanced Peripheral Bus (APB): The APB is part of the AMBA hierarchy of buses and is optimized for minimal power consumption and reduced interface complexity. The AMBA APB appears as a local secondary bus that is encapsulated as a single AHB or ASB slave device. APB provides a low-power extension to the system bus which builds on AHB or ASB signals directly. The APB bridge appears as a slave module which handles the bus handshake and control signal retiming on behalf of the local peripheral bus. By defining the APB interface from the starting point of the system bus, the benefits of the system diagnostics and test methodology can be exploited.

The AMBA APB should be used to interface to any peripherals which are low bandwidth and do not require the high performance of a pipelined bus interface. The latest revision of the APB[6,7] is specified so that all signal transitions are only related to the rising edge of the clock. This improvement ensures the APB peripherals can be integrated easily into any design flow. These changes to the APB also make it simpler to interface it to the new AHB. An AMBA APB implementation typically contains a single APB bridge which is required to convert AHB or ASB transfers into a suitable format for the slave devices on the APB. The bridge provides latching of all address, data and control signals, as well as providing a second level of decoding to generate slave select signals for the APB peripherals.

IV. COMPARISON OF BUSES

Following table shows the comparison among the AMBA buses:

AHB	ASB	APB
High performance	High performance	Low power
Pipelined operation	Pipelined operation	Latched address and control
Multiple bus masters	Multiple bus masters	Simple interface
It consists of master, slave, arbiter decoder	It consists of master, slave, arbiter decoder	It consist of APB bridge and slave

Table 1: Comparison of buses

V. PROPOSED WORK

As discuss above, APB is good choice for implementing Advanced Microcontroller Bus Architecture by using HDL.

VI. CONCLUSION

Implementation of proposed work i.e. AMBA APB prvides the basic peripheral macro cell communications infrastructure as a secondary bus from the higher bandwidth pipelined main system bus .Such peripherals typically:

(i) Have interfaces which are memory-mapped registers
(ii) Have no high-bandwidth interfaces
(iii) Are accessed under programmed control.

REFERENCES

[1] AMBA specification, version 2.0.

[2] Akhilesh kumar and Richa Sinha, "design and verification analysis of ABP3 protocol with coverage "Inaternational journal of advance in engineering and Technology vol. 1 issue 5 pp.310-317,Nov 2011.

[3] Priyanka Gandhani, Charu Patel " Moving from AMBA AHB to AXI Bus in SoC Designs: A Comparative Study" Int. J Comp Sci. Emerging Tech Vol-2 No 4 ,pp.476-479 August, 2011.

[4] Vani. R. M. and Roopa. M "Design of AHB2APB Bridge for different phase and Frequency" International Journal of Computer and Electrical Engineering, Vol. 3, No. 2,pp. April, 2011.

[5] Wang Zhonghai,Ye Yizheng,Wang Jinxing, and Yu Mingyan, "Designing AHB/PCI Bridge,"in Proceedings of 4th International Conference on ASIC, Oct 2001,pp.578-580.

[6] Jaehoon Song, Student member, IEEE, Hyunbean Yi, Member,IEEE, Juhee Han, and Sungju Park, Member, IEEE,"An Efficient SOC Test Technique by Reusing On/Off-Chip Bus Bridge"IEEE Transcactions on Circuits and Systems-I: Regular Papers, Vol,56,No.3,March2009.

[7] Sangik Choi and Shinwook Kang, Mobile SamsungElectronics Co.,Ltd, "Implementation of an On-Chip Bus Bridge between Heterogeneous Buses with Different Clock Frequencies".IEEE, IDEAS'05,1098-8068/2005.

AUTHORS

1 **First Author:** Ms. Radhika Koti
Student M.Tech (VLSI)
Priyadarshini College of Engineering
Nagpur – India
Email ID: kotiradhika10@rediffmail.com

2 **Second Author:** Ms. Divya Meshram
Lecturer, M.Tech
Priyadarshini College of Engineering
Nagpur – India
Email ID: divyameshram@gmail.com