A Verilog Model of Universal Scalable Binary Sequence Detector

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Abstract- This paper presents a Verilog based Universal Sequence Detector, which will be able to detect a binary sequence, from a sequence of inputs. The Sequence Detector looks for some specified sequence of inputs and outputs 1, whenever the desired sequence has found. The sequence detector is like a lock which unlocks (outputs 1), only when a combination appears. Coding of design is done in Verilog HDL and the design is tested and simulated in ModelSim Simulator and is implemented on Xilinx Virtex 4 XC4VFX12 FPGA device.

Index Terms- FPGA, Xilinx, ModelSim, Sequence Detector, HDL.

I. INTRODUCTION

In a computer network like Ethernet, digital data is sent one bit at a time, at a very high rate. Such a movement of data is commonly called a bit-stream. One characteristic is unfortunate, particularly that any one bit in bit stream looks identical to many other bits. Clearly it is important that a receiver can identify important features in a bit stream. As an example, it is important to identify the beginning and ending of a message. This is the job of special bit sequences called flags. A slag is simply a bit sequence that serves as a marker in the bit stream. To detect a flag in bit stream a sequence detector is used.

In this paper we have developed a universal sequence detector. The design implemented in Verilog HDL Hardware Description Language. It was simulated using ModelSim simulator and then is tested for the validation of the design on Virtex 4 XC4VFX12 FPGA.

A) Field Programmable Gate Array

Field Programmable Gate Array (FPGA) is a reconfigurable hardware platform useful for the implementation of high digital functions. Using fixed point, parallel computational structures, FPGA provides computational speeds as much as 100 times greater than those possible with Digital Signal Processors (DSP). The extremely fast computational capability of FPGAs allows a few microseconds for real-time computation of algorithms in spite of their complexities. Furthermore, as DSPs, FPGAs are very low cost components. Virtex 4 XC4VFX12 FPGA's are ideal for low-cost, high-volume applications and are targeted as replacements for fixed-logic gate arrays. The Virtex 4 XC4VFX12 FPGA is not only available for a very low cost, but it integrates many architectural features associated with high-end programmable logic. This combination of low cost and integrated features has made it an ideal replacement for ASICs (Application Specific Integrated Circuits).

B) ModelSim Simulator

ModelSim simulator is a Mentor Graphics product which is capable to simulate various programs of Hardware Description Languages. It combines single kernel simulator (SKS) technology with a unified debug environment for Verilog, VHDL, and SystemC. The combination of industry-leading, native SKS performance with the best integrated debug and analysis environment make ModelSim the simulator of choice for both ASIC and FPGA designs.

II. SYSTEM IMPLEMENTATION

Binary sequences are inserted at the beginning (or end) of the data frame or sub frame emanating from a digital data processor of a space craft. Sequence detectors are used in the detecting equipment on the ground to provide flags which indicate the beginning (or end) of a data block. The sequence detector is in essence an electronic combination lock which is opened for one digit period only when the proper sequence of binary digits is entered. In general sequence detectors can be designed using the state machines. Those detectors which were designed using state machines are limited to detect a particular sequence. As the state machine varies from one required sequence to other, it will be difficult to design a universal detector which will able to detect any sequence of any length.

Universal Scalable Sequence detector design can be achieved if we use a scalable shift register. So we have designed Detector using scalable shift register, which stores the input sequence and compares it with the required sequence to be detected. Scalable register in the sense that, the register facilitates us in storing any number of bits. In general, the required sequence that should be detected is stored in internal register.

Whenever the input binary sequence is applied to the shift register, it takes the sequence bit by bit for every clock cycle and shifts to the right in the next clock cycle. If the sequence resting in the shift register matches with the required sequence, present in the internal register, an output pulse will be generated, acknowledging the user about the detection of the sequence.

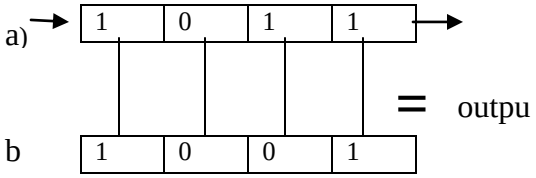

Figure1: Representation of Detection of Required Sequence

The representation of detection of required sequence is shown in the above figure. The first block a) containing four memory spaces is the scalable shift register and the second block b) containing four memory spaces represent an internal register. Here in this case the sequence to be detected is 1001, which will be stored in internal register. The Scalable register takes the size of internal register. The major sequence from which the require sequence is to be detected will be carried from the LSB of the shift register to the MSB of it. Whenever the binary contents of the shift register matches with that in the Internal register, an output pulse will be generated. Similarly we can be able to detect any sequence of any length. The sequence to be detected will be stored in the Internal register, shift register of same memory will be generated and then compared, finally detecting the required sequence.

III. SIMULATION RESULTS

The design is simulated in ModelSim PE student Edition Figure 3 shows the timing waveform of the design obtained with ModelSim PE student Edition Simulator for a 8 bit sequence. Design is implemented on Xilinx Virtex 4 XC4VFX12 FPGA device. The top level of RTL schematic obtained by synthesizing the design in Xilinx is shown in Figure 2 and the pins are described in Table 1.

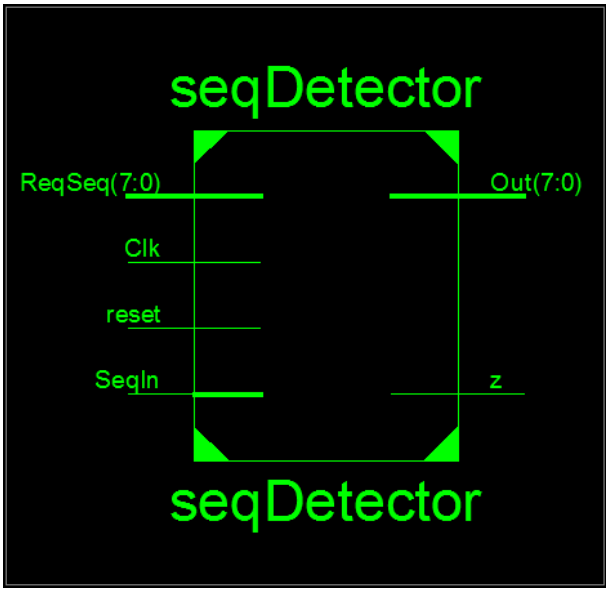

Figure 2: Top level block diagram of universal Scalable binary sequence detector

Table 1: Pin Description

Input Signal	**Description**
ReqSeq(7:0)	Required Sequence to be detected here in this example it is of 8 bit
Clk	System Clock signal input
reset	Reset signal input
Seqin	Input binary sequence from which required sequence to be detected
Output signal	**Description**
Out(7:0)	Shift register output at every clock
z	The Output if sequence is detected

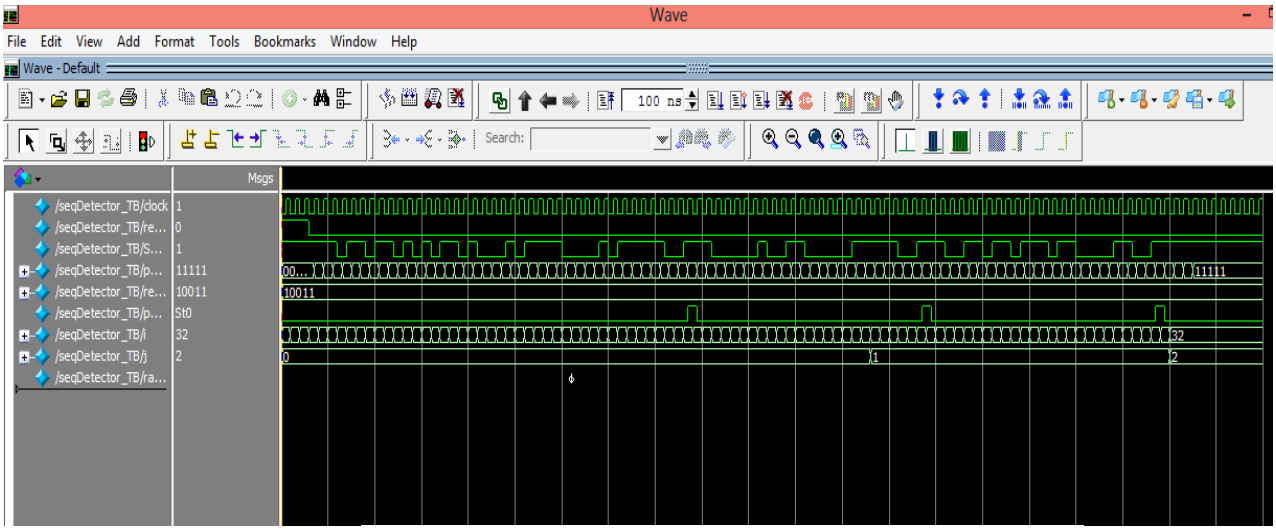

Figure 3: Simulation results obtained from Modelsim simulator

The percentage utilization of FPGA in terms of number of slices, number of flip-flops and number of Look up tables (LUTs) are evaluated .The Device utilization summary obtained from Xilinx is shown in Figure 4

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Flip Flops	41	10,944	1%
Number of 4 input LUTs	62	10,944	1%
Number of occupied Slices	52	5,472	1%
Number of Slices containing only related logic	52	52	100%
Number of Slices containing unrelated logic	0	52	0%
Total Number of 4 input LUTs	93	10,944	1%
Number used as logic	62		
Number used as a route-thru	31		
Number of bonded IOBs	20	320	6%
IOB Flip Flops	1		
Number of BUFG/BUFGCTRLs	1	32	3%
Number used as BUFGs	1		
Average Fanout of Non-Clock Nets	2.46		

Figure 4: Device utilization summary

The complete schematic of the design showing all the inputs and outputs at the inside level is shown in Figure 5. In this example it detects the binary sequence of 8 bits. It includes AND gates, Magnitude comparators, D flipflops , NOT gates.

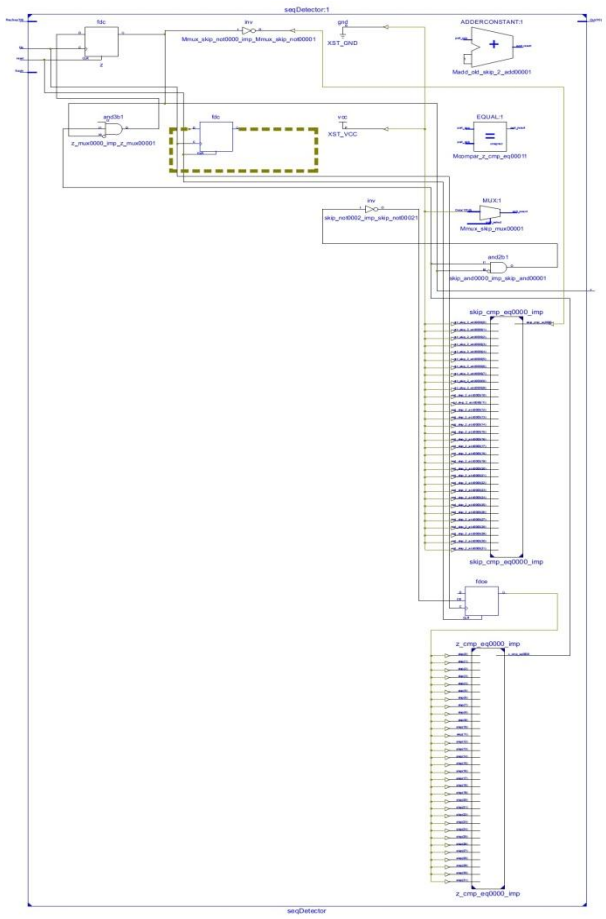

Figure 5: Internal view block diagram of universal scalable binary sequence detector

IV. CONCLUSION

In this paper we have developed a universal scalable binary sequence detector. The design implemented in Verilog HDL Hardware Description Language. It was simulated using ModelSim simulator and then is tested for the validation of the design on Virtex 4 XC4VFX12 FPGA board and the design is proved to be efficient.As the name suggests it is sacalabe and can be used to detect the sequence of any length within the storage capacity of register.

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