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Design and Analysis of Low Power Pulse Triggered Flip-Flop

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Abstract- Practically, clocking system like flip-flop (FF) consumes large portion of total chip power. In this paper, a novel low-power pulse-triggered flip-flop (FF) design is presented. Pulse- triggered FF (P-FF) has been considered as a popular alternative to the conventional master –slave based FF in the applications of high speed. First, a simple two-transistor AND gate design is used to reduce the circuit complexity. Second, a conditional pulse-enhancement technique is devised to speed up the discharge along the critical path only when needed. As a result, transistor sizes in delay inverter and pulse-generation circuit can be reduced for power saving. The maximum power saving against rival designs is up to 39.4%.Compared with the conventional transmission gate-based FF design; the average leakage power consumption is also reduced by a factor of 3.52.

Index Terms *– Flip-flop, low power, pulse-triggered*

I. INTRODUCTION

Flip-flops (FFs) are the basic storage elements used extensively in all kinds of digital designs. In particular, digital designs now-a-days often adopt intensive pipelining techniques and employ many FF-rich modules. It is also estimated that the power consumption of the clock system, which consists of clock distribution networks and storage elements, is as high as 20%–45% of the total system power. Traditional master-slave flip-flops are made up of two stages, one master and one slave and they are characterized by their hard-edge property. Alternatively, pulse-triggered flip-flops reduce the two stages into one stage and are characterized by the soft edge property. Pulse-triggered FF (P-FF) has been considered a popular alternative to the conventional master–slave based FF in the applications of high-speed operations. Besides the speed advantage, its circuits simplicity are also beneficial to lowering the power consumption of the clock tree system. The circuit complexity of a P-FF is simplified since only one latch, as opposed to two used in conventional master–slave configuration, is needed. P-FFs also allow time borrowing across clock cycle boundaries and feature a zero or even negative setup time. Depending on the method of pulse generation, P-FF designs can be classified as implicit or explicit. In an implicit-type P-FF, the pulse generator is a built-in logic of the latch design and no explicit pulse signals are generated. In an explicit-type PFF, the designs of pulse generator and latch are separate. Implicit pulse generation is often considered to be more power efficient than explicit pulse generation. In this paper, we will present a novel low-power implicit-type P-FF design featuring a conditional pulse-enhancement scheme. Three additional transistors are employed to support this feature. In spite of a slight increase in total transistor count, transistors of the pulse generation logic benefit from significant size reductions and the overall layout area is even slightly reduced.

II. IMPLICIT-TYPE P-FF DESIGN WITH PULSE CONTROL SCHEME

A.Conventional Implicit-Type P-FF Designs

1)ip-DCO: ip-DCO is known as the implicit data close to output. It is an implicit type flip-flop. In this method the pulse is generated inside the flip-flop. A state-of-the-art P-FF design, named ip-DCO, is given in Fig.1. It contains an AND logic-based pulse generator and a semi-dynamic structured latch design. Semi-Dynamic Flip-Flop is a high performance flip-flop because of its small delay and simple topology. It is measured to be one of fastest flip-flops today.

Inverters I5 and I6 are used to latch data and inverters I7 and I8 are used to hold the internal node X. The pulse generator takes complementary and delay skewed clock signals to generate a transparent window equal in size to the delay by inverters I1-I3. Two practical problems exist in this design. First, during the rising edge, nMOS transistors N2 and N3 are turned on. If data remains high, node X will be discharged on every rising edge of the clock. This leads to a large switching power.

2)MHLFF: The modified hybrid latch flip-flop is known as MHLFF and this is an type of implicit type flip-flop. MHLFF shows an improved P-FF design in fig.2. It employs a static latch structure. A static latch can remember as long as gate power is supplied. It uses feed-back to remember, rather than depending on the charge on a capacitor. Node X is no longer precharged periodically by the clock signal. A weak pull-up transistor P1 controlled by the FF output signal Q is used to maintain the node level at high when Q is zero.

This design eliminates the unnecessary discharging problem at node. However, it encounters a longer Data-to-Q (D-to-Q) delay during "0" ,"1" transition because node is not pre-discharged. Larger transistors N3 and N4 are required to enhance the discharging capability. Another drawback of this design is that node becomes floating when output Q and input Data both equal to "1". Extra DC power emerges if node X is drifted from an intact"1".

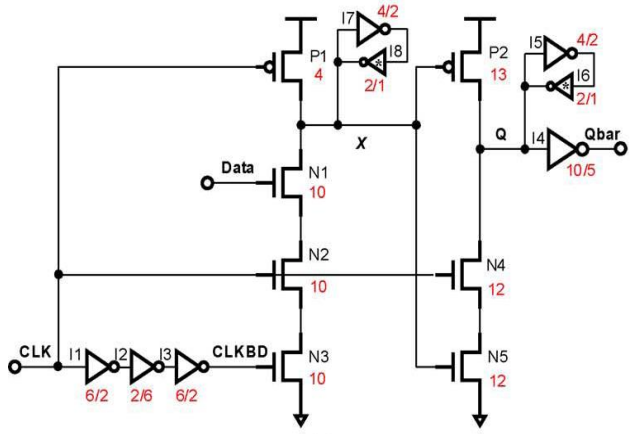

Figure.1. ip-DCO

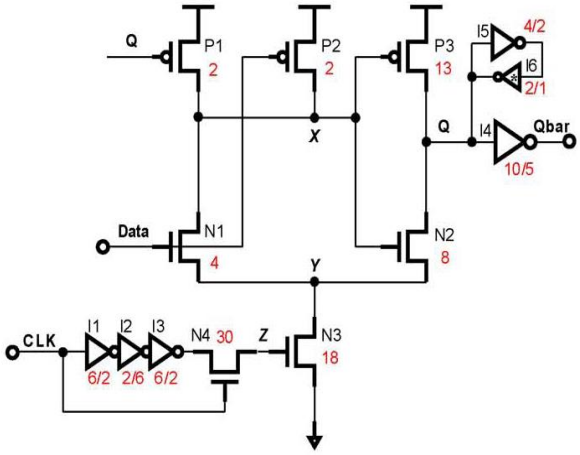

Figure.2. MHLFF

3)SCCER: SCCER is known as the single ended conditional capturing energy recovery P-FF. It is a refined low power P-FF design using a conditional discharged technique. This technique is also used to present a new flip-flop Conditional Discharge flip-flop (CDFF). CDFF use a pulse generator which is suitable for double edge sampling. CDFF has two stages. First is responsible for capturing the Low-to-High transition and second stage captures the High-to-Low input transition. In this SCCER design, the keeper logic is replaced by a weak pull up transistor P1 in conjunction with an inverter I2 to reduce the load capacitance of node. The discharge path contains nMOS transistors N2 and N1 connected in series. In order to eliminate superfluous switching at node, an extra nMOS transistor N3 is employed. Since N3 is controlled by Q_fdbk, no discharge occurs if input data remains high.

The worst case timing of this design occurs when input data is "1" and node is discharged through four transistors in series, i.e., N1 through N4, while combating with the pull up transistor P1. A powerful pull-down circuitry is thus needed to ensure node can be properly discharged. This implies wider N1 and N2 transistors and a longer delay from the delay inverter I1 to widen the discharge pulse width.

III. PROPOSED P-FF DESIGN

Fig. 4 shows the proposed design. The proposed design, adopts two measures to overcome the problems associated with existing P-FF designs. The first one is reducing the number of nMOS transistors stacked in the discharging path. The second one is supporting a mechanism to conditionally enhance the pull down strength when the input data is "1." As opposed to the transistor stacking design in Fig. 1 and Fig. 3, transistor N2 is removed from the discharging path. Transistor N2, in conjunction with an additional transistor N3, forms a two-input pass transistor logic (PTL)-based AND gate to control the discharge of transistor N1. Pass transistors require lower switching energy to charge up a node, due to the reduced voltage swing.

In SCCER design, the discharge control signal is driven by a single transistor. Parallel conduction of two nMOS transistors (N2and N3) speeds up the operations of pulse generation. Thus the number of stacked transistors along the discharging path is reduced. To enhance the discharging condition, transistor P3 is added. When the FF output Q changes from 0 to 1 the conditional pulse enhancement technique effectively takes place. Thus this leads to the better power performance compared to the indiscriminate pulse enhancement approach.

The post layout simulations on various P-FF were conducted to obtain the performance figure of the proposed design. These designs include three flip-flops namely ip-DCO, MHLFF and SCCER. And those designs are discussed above. The target technology is the UMC 90-nm CMOS process. The operating condition used in simulations is 500 MHz/1.0V.

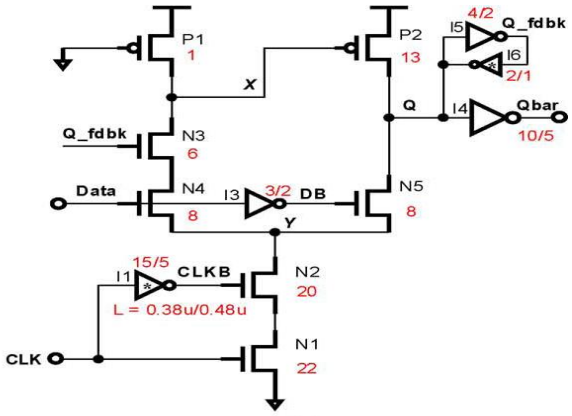

Figure.3. SCCER

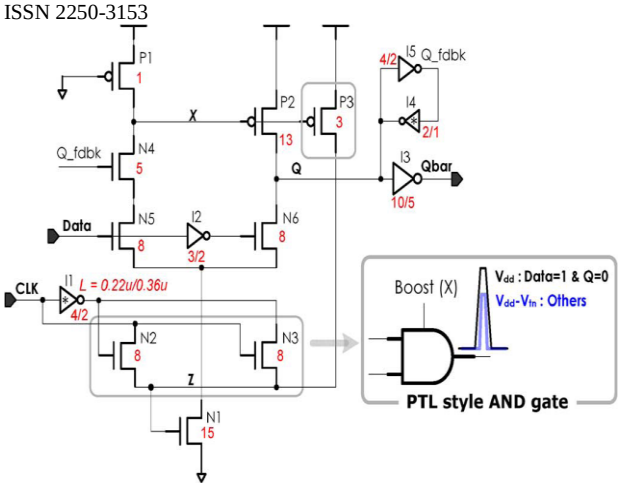

Figure.4. Schematic of the proposed P-FF design with pulse control scheme

IV. Simulation Results

The simulation results of above designs are shown below in the Fig. 5 to Fig. 8.

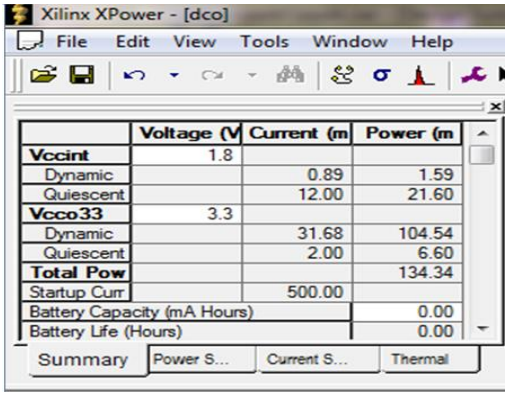

Figure.5. Power consumed by ip-DCO

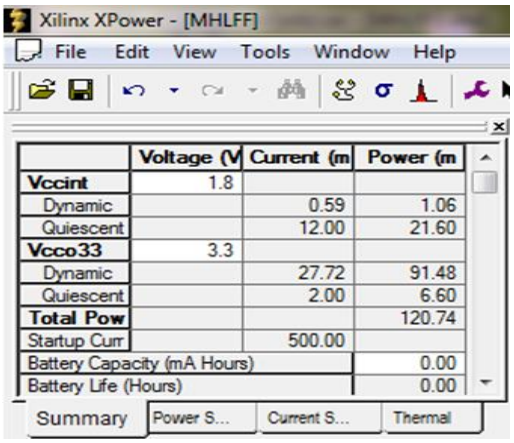

Figure.6. Power consumed by MHLFF

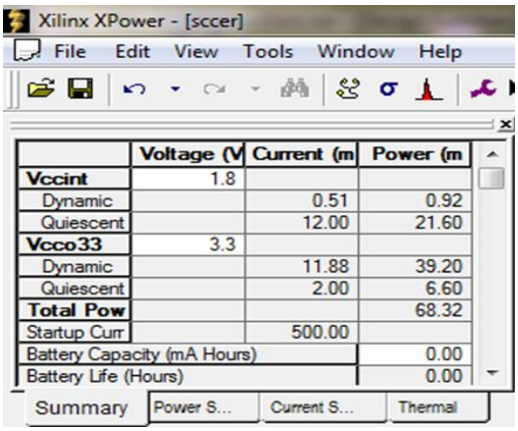

Figure.7. Power consumed by SCCER

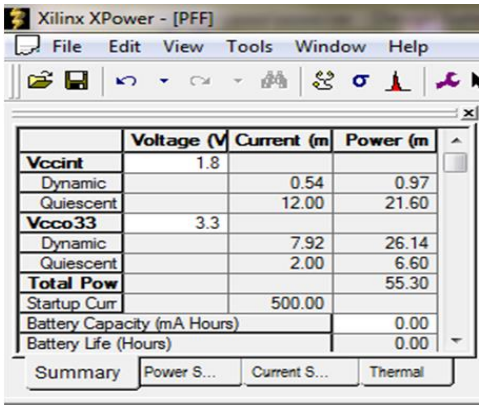

Figure.8. Power consumed by P-FF

The power consumed by the ip-DCO is 134.34mW, MHLFF is 120.74mW, SCCER is 68.32mW and P-FF is 55.3mW.By comparing the above results, we came to know that power consumption of P-FF design is low.

Table.I. Power Comparision

FF	TOTAL ESTIMATED POWER CONSUMPTION P(mW)
ip- DCO	134.34
MHLFF	120.74
SCCER	68.32
P-FF	55.3

V. Conclusion

In this paper, we devise a novel low-power pulse-triggered FF design. This was successfully done by reducing the number of transistors stacked along the discharging path by incorporating

a PTL-based AND logic. The table 1 has been added to verify that the proposed design will be better compared to the existing design like ip-DCO, MHLLF, SCCER.

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