Low Power Techniques for High Speed FPGA

P.A.Kamble *, Prof M.B.Mali**

* Sinhgad College of Engineering, Vadagaon (Bk), Pune.
E-mail: kamble.prachi@gmail.com
** Sinhgad College of Engineering, Vadagaon (Bk), Pune.

Abstract- The motive of this work is to design on chip efficient low power techniques using VHDL coding. Serial links in network on chip provide many advantages in terms of crosstalk, skew, area cost, clock synchronization, and wiring difficulty when compared to multi-bit parallel data transmission. The proposed a novel coding technique reduces the number of transitions and hence reduces transmission energy on the serial wire. Also low power consumption is achieved by using the mux-tree based round robin scheduler. A scheduler (or arbiter) is needed when more than two input packets from different input ports are destined for the same output port at the same time.

Index Terms- FPGA, mux tree based round robin scheduler, parallel to serial transmission, low energy coding on chip serial link,

I. INTRODUCTION

The on chip inter-modular communications become congested, as Systems-on-Chip (SoC) integrate an ever growing number of modules and modules may require serial interfaces, similar to the parallel to serial inter-chip interconnects. A multi-bit bus with a global common clock has been widely used as communication architecture for the most of VLSI designs. However, in a high performance SoC and deep-submicron, multi-bit and long bus lines have several problems such as crosstalk, skew, large area and, wiring difficulty. It is difficult to increase the frequency of global clock due to jitter or skew on multi-bit lines because of data on the bus must be synchronized with the common clock. In multimedia SoC the area cost of the wide-bit bus is serious. However the noise and data dependent signal delay is occurred because of the crosstalk between adjacent bus lines. Multi bit bus communication performance is bounded by available clock rate, delay uncertainty, and clock skew due to layout geometries, process variations, and crosstalk noise. Therefore parallel link with a global clock will reach its limit and make expensive further performance enhancement.

To overcome such problems, source synchronous serial communication is one of the key technologies. In serial communication due to less communication lines it occupies less area. The source-synchronous serial communication uses a sideband strobe signal along the serial data line. The strobe signal is a clock signal but it is activated only when the serial data line is valid. It has an identical wire delay and load with the data line, so that the skew between data and clock is get reduced. Moreover the crosstalk problem can be mitigated by wide spacing of serial lines. In this paper, a serialized low-energy transmission coding method is proposed for on-chip serial communication. This technique is used in a on-chip inter-connection networks, and also high-performance memory I/O recently.

There were many researches on low-power bus coding but they are mostly for parallel bus. As the number of subsystems on a chip and the die sizes increase, the power consumed by the interconnection structures takes significant portion of the overall power-budget. A pro-posed serialized low-energy transmission (SILENT) coding technique decreases the number of transitions on a serial data wire to reduce the power consumption of wire and transmitter.

In proposed work mux tree based round-robin scheduler and serialized low-energy transmission coding technique are used. A scheduler is needed when more than two input packets from different input ports are destined for the same output port at the same time. Among a number of scheduling algorithms, a mux tree based round-robin algorithm is most widely used in on-chip networks due to its lightness and fairness.

II. SYSTEM DESIGN

The proposed project consist of mux tree based round robin scheduler, serialized low-energy transmission coding technique, serial memory, parallel memory and peripheral unit.fig 1 illustrates the block diagram of proposed project.

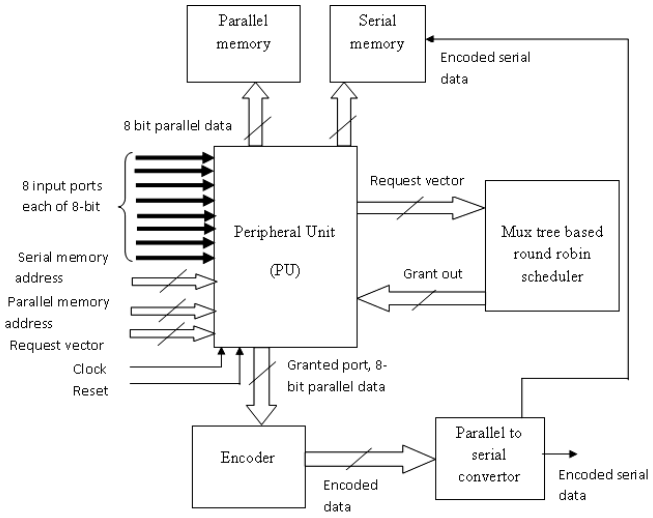

Fig. 1. Block diagram of proposed project

The request vector and eight input-ports are given as an input to the peripheral unit. Peripheral unit take input data of the system and it gives to the respective blocks. Also it provides handshaking signal to the remaining blocks of the system. A request vector is given as an input to the peripheral unit it gives to mux tree based round robin scheduler. The output of scheduler is grant out. Scheduler grants one of the input port if there is multiple input port wants the same output port. The granted input port data is a eight bit parallel data. The granted input port eight bit parallel data is given to the encoder of SILENT coding. The SILENT coding block consists of encoder and serial to parallel converter. The output of encoder is given as an input to the serial to parallel converter. The out of serial to parallel converter is encoded SILENT serial data. The granted input port data is stored in parallel memory at respective given input parallel memory address. Also the encoded serial data is stored at respective given input serial memory address location.

III. MUX TREE BASED ROUND-ROBIN SCHEDULER

The round robin scheduler has rotating pointer that indicates the most recently granted port. A port next to the pointer has the highest priority to be grant. The block diagram of mux tree based round robin scheduler is shown in fig. 2.

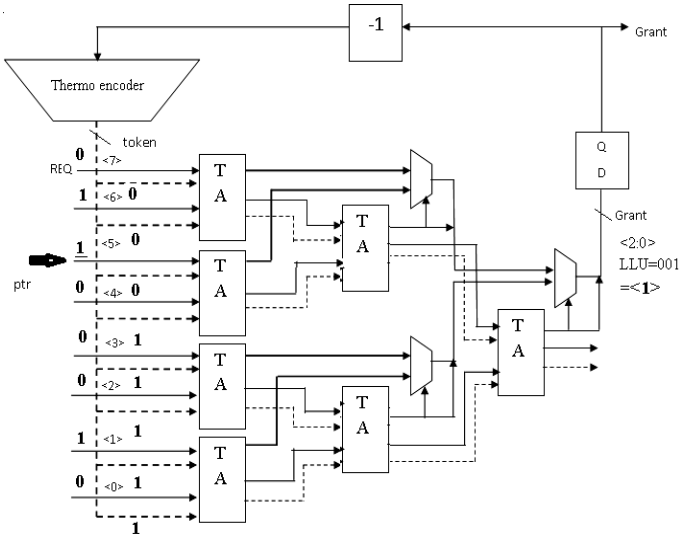

Fig. 2 Block diagram of mux tree based round robin scheduler

TABLE 1
TINY ARBITER (TA)

Upper		Lower		U or L
RQ	TK	RQ	TK	
0	X	0	X	U
1	X	0	X	U
0	X	1	X	L
1	1	1	0	U
1	0	1	1	L
1	0	1	0	U
1	1	1	1	U

The mux tree based round robin scheduler is design for eight input request, as in the proposed project we are using eight input ports. A request from a port having a token acquires higher priority than others. These request and token vectors are inputs of the binary mux tree which is composed of tiny arbiters (TA) at each node. Each tiny arbiter selects one of two ports, upper one or lower one, based on a table I. The fig. 3 shows the RLT schematic of mux tree based round robin scheduler. For example, request vector<7:0> = 01100010 is shown in Fig. 2 where underline means a current position of the pointer. Then, port<4> has the highest priority and the lower group of port<4:0> has higher priority than upper group of port<7:5>. This information is given by a thermo-encoder whose output becomes token <7:0> = 00011111. Therefore, ports <4:0> have their tokens while ports <7:5> do not. A request from a port having a token acquires higher priority than others. These request and token vectors are inputs of the binary Mux-Tree which is composed of tiny arbiters (TA) at each node. Each TA selects one of two ports, upper one or lower one, based on a table shown in table 1. When both of the two requests have no token or both of them have their tokens, TA selects upper port because the pointer rotates in decreasing order. Then, the TA forwards the winners request and token to its parent node. Then one of two children UorL bits is selected by 2:1 MUX based on their parents UorL bit. The selected child-UorL bit and its parent-UorL bit are concatenated and propagate to its grandparent node. By the successive propagation up to the root node, the granted port number, grant<2:0> is determined finally.

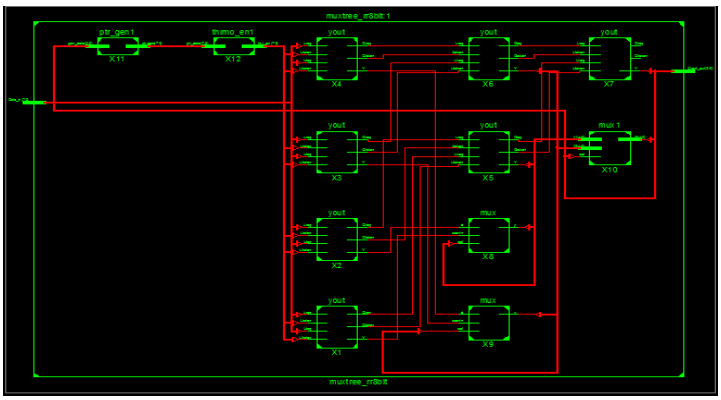

Fig. 3 RTL schematic of mux tree based round robin scheduler

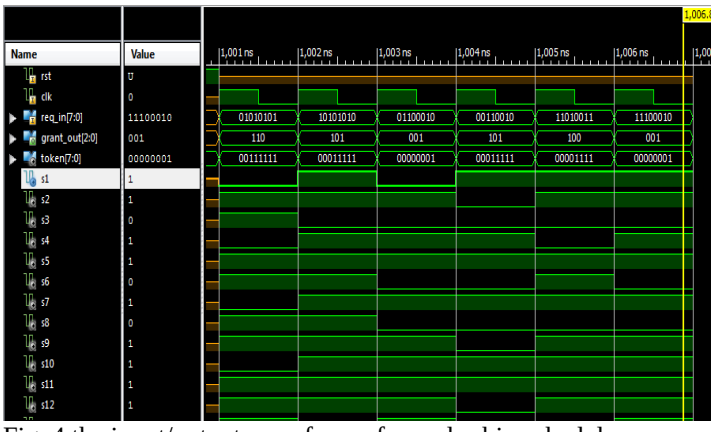

Fig. 4 the input/output waveform of round robin scheduler.

The fig. 4 shows the input/output waveform of round robin scheduler.

IV. LOW ENERGY CODING ON ON-CHIP SERIAL LINK

Many parallel bus coding methods have been proposed to reduce the switching power on the data or address bus between memories and a processor. However, such conventional parallel bus coding methods cannot be employed in the serial bus. Therefore, we propose a serialized low-energy transmission (SILENT) coding technique to minimize the transmission energy on the serial wire by using the data correlation properties. We first introduce Many parallel bus coding methods have been proposed to reduce the switching power on the address or data bus between a processor and memories [5-6]. However, such conventional parallel bus coding methods cannot be employed in the serial bus. Therefore, we propose a serialized low-energy transmission (SILENT) coding technique to minimize the transmission energy on the serial wire.

(a) Original parallel data

	t0	t1	t2	t3	t4
b[7]	0	0	0	0	0
b[6]	1	1	1	1	1
b[5]	0	0	0	0	0
b[4]	1	1	1	1	1
b[3]	0	0	0	0	0
b[2]	0	0	0	1	1
b[1]	0	1	1	0	0
b[0]	1	0	1	0	1
# of tr.		2	1	3	1

CODING

(b) Encoded parallel data

	t0	t1	t2	t3	t4
B[7]	0	0	0	0	0
B[6]	1	0	0	0	0
B[5]	0	0	0	0	0
B[4]	1	0	0	0	0
B[3]	0	0	0	0	0
B[2]	0	0	0	1	0
B[1]	0	1	0	1	0
B[0]	1	1	1	1	1

SERIALIZIN

SERIALIZIN

(c) Conventional serial data

	Serial data								# of tr.
t	0	1	0	1	0	0	0	1	5
t1	0	1	0	1	0	0	1	0	7
t2	0	1	0	1	0	0	1	1	5
t3	0	1	0	1	0	1	0	0	7
t4	0	1	0	1	0	1	0	1	7

(d) Encoded serial data

	Serial data								# of tr.
t	0	1	0	1	0	0	0	1	5
t1	0	0	0	0	0	0	1	1	2
t2	0	0	0	0	0	0	0	1	2
t3	0	0	0	0	0	1	1	1	2
t4	0	0	0	0	0	0	0	1	2

Fig. 5. (a) original data words; (b) encoded data words; (c) conventional serial data with 31 transitions; (d) encoded serial data with 13 transitions.

In serial communication, the switching activity factor of a serial wire is different from that of parallel wires. The difference in activity factor strongly depends on the transacted data patterns. In this coding, only the differences between successive parallel data words are encoded as 1's. The encoding algorithm is expressed as follows:

b (t) [n-1:0]: n-bit data word from a sender at time t
B (t) [n-1:0]: n-bit encoded data word at time t

The encoder works as follows:

$$B(t)[i] = b(t)[i] \quad b(t-1)[i] \qquad \text{for } i = 0 \sim n-1 \qquad (1)$$

The encoded words, B (t), are equivalent to the displacement or the difference between successive data words. By serializing the encoded data words, the frequency of the appearance of zeros on the wire increases because of the correlation between the successive data words, b(t)
. Figure 4 shows an example for the advantage of this coding method. All bits from B[7] to B[3] become zeros after these data words are encoded because those bits do not change with time. Serializing these encoded words reduces the number of transitions of the serial wire as shown in Figure 4(d) and the wire looks silent
. In this example, a conventional serial wire without the SILENT coding, shown in Figure 4(c), has three times as many transitions from t+1 to t+4. By reducing the number of transitions on the serial wire, the transmission energy can be saved proportionally. After deserialization at the receiver end, the decoder works as follows:

$$b(t)[i] = B(t)[i] \; b(t-1)[i] \qquad \text{for } i = 0 \sim n-1 \qquad (2)$$

The original data word from a sender unit, b(t), can be recovered by XORing the encoded word, B(t), and a previously decoded word, b(t-1).

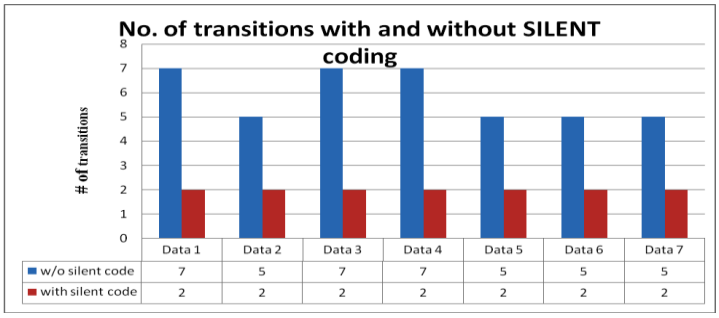

Fig. 6. Number of transitions with and without SILENT coding

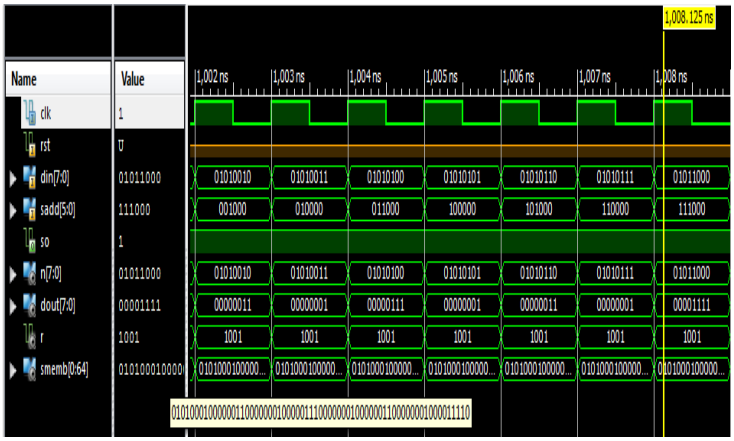

Fig. 7. Input / output waveform of proposed work.

V. CONCLUSION

In this paper, we have proposed a mux tree based round robin scheduler and low-energy on chip serial communications technique for high speed fpga. The on chip serial coding technique reduces the number of transitions on serial wires using the data correlation between successive data words. We show that the coding method saves significant amount of the communication energy by reducing the number of transitions. Mux tree based round robin scheduler is also reducing the power consumption in network layer. We implemented a low power technique for high speed fpga.

ACKNOWLEDGMENT

I would like to express my true sense and sincerest gratitude, to our principal, Dr.S.D.Lokhande, for providing necessary facilities towards carrying out this work. We acknowledge the diligent efforts of our Head of the Department Dr. M.B. Mali for his dynamic and valuable guidance and keep interest in the project and I am grateful to himfor his constant encouragement in the project work.

REFERENCES

[1] International Technology Roadmap for Semiconductors [Online]. Available: http://public.itrs.net

[2] W. Dally *et al.*, "Route packets, not wires: On-chip interconnection networks," in *Proc. Des. Autom. Conf.*, Jun. 2001, pp. 684–689.

[3] L. Benini *et al.*, "Networks on chips: A new SoC paradigm," *IEEE Computer*, vol. 36, no. 1, pp. 70–78, Jan. 2002.Si. Liao, Max. W. K. Law and Albert C. S. Chung, "Dominant Local Binary Patterns for Texture Classification," *IEEE transactions on image processing*, vol 18, no 5, May 2009.

[4] D. Bertozzi *et al.*, "Xpipes: A network-on-chip architecture for giga scale system-on-chip," *IEEE Circuits Syst. Mag.*, vol. 4, no. 2, pp. 18–31, 2004.

[5] E. Rijpkema *et al.*, "Trade offs in the design of a router with both guaranteed and best-effort services for networks on chip," in *Proc. Des., Autom. Test Europe Conf.*, Mar. 2003, pp. 350–355.

[6] V. Nollet *et al.*, "Operating-system controlled network on chip," in *Proc. Des. Autom. Conf.*, Jun. 2004, pp. 256–259.

[7] J.-S. Kim *et al.*, "On-chip network based embedded core testing," in *Proc. IEEE Int. SoC Conf.*, Sep. 2004, pp. 223–226.

[8] S.-J. Lee *et al.*, "An 800 MHz star-connected on-chip network for application to systems on a chip," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2003, pp. 468–469.

[9] M. Taylor *et al.*, "A 16-issue multiple-program-counter microprocessor with point-to-point scalar operand network," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2003, pp. 170–171.

[10] K. Lee *et al.*, "A 51 mW 1.6 GHz on-chip network for low-power heterogeneous SoC platform," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2004, pp. 152–153.

[11] H. Wang *et al.*, "A technology-aware and energy-oriented topology exploration for on-chip networks," in *Proc. Des., Autom. Test Europe Conf.*, Mar. 2005, pp. 1238–1243.

[12] BONE: Network-on-Chip Protocol [Online]. Available:http://ssl.kaist.ac.kr/ocn

AUTHOR

Prachi Arun Kamble – She received B.E. degree in Electronics and Telecommunication from Solapur Univrsity, Maharashtra, India in 2008, Embedded System course certificate in 2008-09 and doing post graduation in VLSI and Embedded System Design from Sinhagad College of Engineering, Vadagaon , Pune, University of Pune, Maharashtra, India. Email address: kamble.prachi@gmail.com, prachipol2812@gmail.com, 8806038283.