

A Monotonic Digitally Programmable Delay Element for Low Power VLSI Applications

S.Jayasudha*, B.Ganga Devi**

Department of Electronics and Communication Engineering,
P.A. College of Engineering and Technology, Coimbatore-642 002, India

Abstract-Digitally programmable delay elements (DPDE) are required to be monotonic and low power. A low power digitally programmable delay element (DPDE) with monotonic delay characteristics is proposed and a dynamic current mirror together with a feedback technique enables a current-on-demand operation. The dynamic power is made proportional to the delay with a maximum of $25\mu\text{W}$ and static power is eliminated. DPDE is implemented with two new designs of CMOS digitally controlled oscillators (DCO). First design has been implemented with one driving strength controlled delay cell and with two NAND gates used as inverters. The second design with one delay cell and by two NOR gates is presented.

Index Terms-Delay element, dynamic current mirror, Current-Starved Inverter, monotonic, Digitally Controlled Oscillator (DCO)

I. INTRODUCTION

Delay elements with programmability are often solicited in several high performance VLSI systems to control the rising/falling edge of a desired signal. A continuous voltage can be used to manipulate the delay [8]. However, it is sometimes desirable to vary the delay digitally. Presently, low power Digitally Programmable Delay Elements (DPDE) play a key role in many applications such as Digitally Controlled Oscillators (DCOs), Digital Delay Locked Loops (DDLs), All Digital Phase Locked Loops (ADPLLs), microprocessors and memory circuits.

Several types of digitally controlled delay elements have been reported. The DPDE based on the current-starved inverter is one of the most popular because of its low power consumption. However, charge sharing introduces non-monotonic delay with respect to increasing input digital code. A Current mirror based DPDE that provides monotonic delay and maintains low sensitivity to temperature variation was presented. One main advantage of the delay element is finding the input vector for a specific delay is straightforward.

The architecture, however, dissipates considerable static power and the direct path currents are not well managed.

This paper describes a power efficient DPDE architecture where a dynamic current mirror together with a feedback technique is used to provide current only when needed. This paper examines some of the most classical digitally programmable delay elements. The new delay element and DCO is presented while simulation characterization is given.

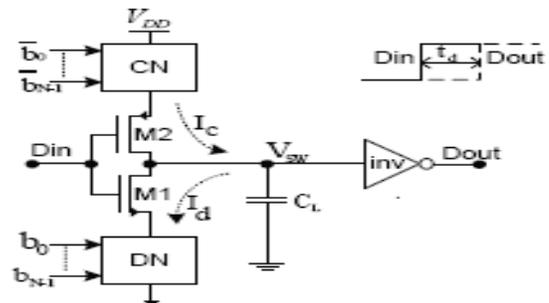


Figure 1 Basic Concept of DPDE

II. DIGITALLY PROGRAMMABLE DELAY ELEMENT

Figure 1 depicts the basic concept of a DPDE. It consists of load capacitor C_L , charging network CN that provides charging current I_c , discharging network DN that provides discharging current I_d , an output inverter INV, and an input inverter formed by M1 and M2. The delay, t_d , depends on the load capacitance, (dis)charging current, and the voltage swing across capacitor, V_{sw} , and is given by

$$t_d = (C_L * V_{sw}) / I(1)$$

Delay control is often accomplished by adjusting I, C_L or V_{sw} .

A. Shunt-capacitor based DPDE

Figure 2 is a shunt capacitor based DPDE that was proposed. A digital input code controls the output capacitive load seen by the input inverter. The MOS with source and drain shorted can be used for the capacitors. The technique is quite robust but the use of capacitors is prohibitive in terms of area.

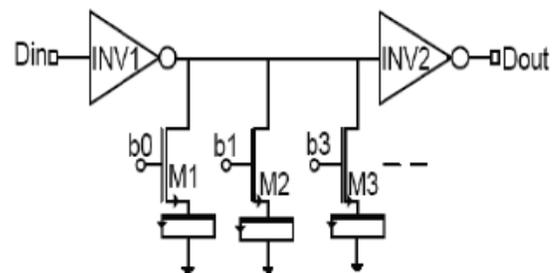


Figure 2 Shunt capacitor based DPDE
B. Variable resistor based DPDE

Figure 3 illustrates another DPDE technique that was proposed. An input code switches a bank of stacked transistors thereby producing varying resistance at the source of M1. Different resistance values produce different discharging currents and hence different delays. Extra coding is however required for the transistor switching.

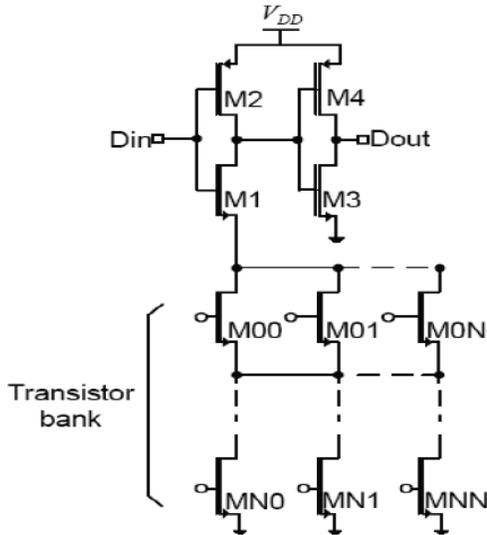


Figure 3 Variable based DPDE

C. CSI based DPDE

A simple technique to digitally program the delay based on current starved inverters was proposed and shown in Figure 4. NMOS control transistors, Mn0, Mn1, Mn2, are connected to the source of M1 and PMOS control transistors, Mp0, Mp1, Mp2, ..., are connected to the source of M2. By an input code, the rising/falling edge can be controlled accordingly. However, due to charge sharing between the capacitance at the output of the input inverter and the capacitance at the source of M1, the delay may not be monotonic. A one to one mapping of input vector to delay is therefore not guaranteed.

This problem was identified and analyzed and a different technique based on a current mirror, shown in Figure 5, was proposed to solve the problem.

The core of the current mirror CSI based DPDE is formed by a current source transistor Msc, current mirror transistors, Mn1, Mn2, input inverter transistors M1, M2 and output inverter transistors, M3 and M4. The delay is controlled through the transistors Mp0~Mp3. The number of transistors can be increased as desired. When Din is low, M1 is off and the output of the input inverter, Vo1, is charged to Vdd. When Din goes high, M1 turns on and starts discharging the capacitance at the output of the input inverter. The discharge current depends on the current through Mn2 which is provided by the current source Msc and control transistors that are switched on. The charge sharing effect is avoided. Though monotonic delay can be achieved, this design suffers from power inefficiency. Firstly, the delay element consumes significant amounts of static power and the dynamic power is not well managed. When the delay element is in reset mode where Din is low, the current source transistor Msc, the current mirror transistor Mn2 and the control transistors are all on resulting in static power dissipation. Nejad suggested

that this static power can be minimized by scaling down the W/L ratios of the controlling, the current source and the current mirror transistors.

However, this might lead to reliability issues. Secondly, as acknowledged, the current starved nature of the structure may cause significant direct currents to flow through the output inverter transistors M3 and M4. This is because, when Din goes high and the discharge current is small, Vo1 may drop at a very slow rate allowing both M3 and M4 to be on simultaneously for a longer time. Moreover, even when the delay event has been completed, the current source transistor Msc continues to provide unnecessary current. As acknowledged the power dissipation resulting from these three sources is very high. The direct current through the output inverter also complicates the derivation of an equation for the delay. The static and direct path currents can be completely eliminated with dynamic current mirror and gate decoupling techniques, respectively.

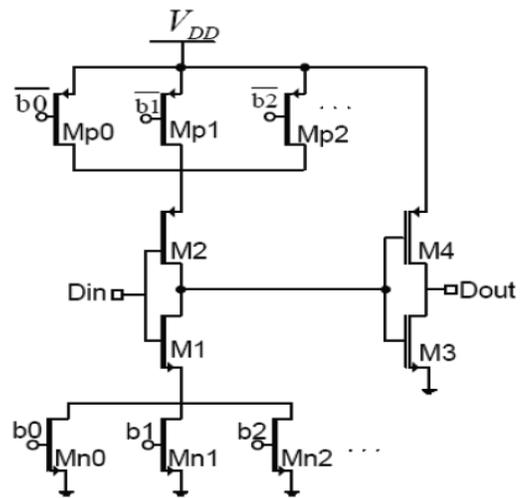


Figure 4 CSI based DPDE

D. PROPOSED DIGITALLY PROGRAMMABLE DELAY ELEMENT

The proposed digitally programmable delay element is shown in Figure 5. The goal is to eliminate static power, reduce dynamic power and improve the current mirror accuracy.

The set of control transistors, Mp0~Mp4 is connected in a similar manner as in Figure 5 so as to preserve the simplicity and monotonic delay characteristics of the delay element. Three major modifications can be identified. The gate of the current source transistor, MCS, is connected to the output of the output transistor. The gates of the NMOS and PMOS transistors of the output inverter are separately controlled. The NMOS transistor, M3 is controlled by the inverted version of Din while the PMOS is still controlled by the output of the input inverter. Another modification is in the current mirror. The NMOS switch of the input inverter, M1, is placed at the source of the current mirror transistor, Mn1, rather than the drain. Another switch transistor, M5, is placed at the source of the other current mirror transistor Mn2.

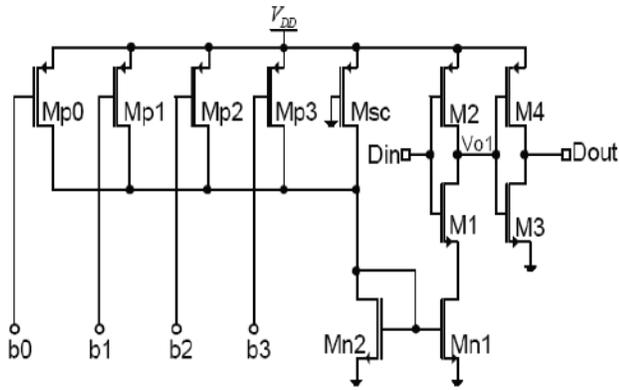


Figure 5 Modified CSI based DPDE

When Din is low, M1, M5 and M6 are switched off. M2 is switched on followed by M7 and M3. Since M2 has to switch on before M7, the gate voltage of M3 lags behind that of M4. Therefore, M4 switches off before M3 switches on and direct path currents through these transistors are eliminated. The source transistor Msc is switched on since M3 pulls its gate to a low voltage. When Din turns high, M1, M5, M6 are switched on while M2, M7 and M3 are switched off. The delay element then operates just as the conventional type. However, since M3 turns off before M4 turns on, direct current during this phase is also eliminated. Moreover, when Dout switches to V_{DD}, current source transistor Msc switches off since it is no longer needed and the current through it is cutoff till Dout goes low again during reset. Another interesting modification worth noting is that, Mn1 and Mn2 are always in saturation when needed. When Din, switches from low to high, the source of Mn1 and Mn2 are at ground voltage giving them sufficient drain-source voltage to remain in saturation. Before Mn1 enters the linear region Dout would have switched to V_{DD}. This allows a more accurate current mirror than that presented in Figure 5 and better predictability of the delay. The input current I_{IN} through Mn2 is given as

$$I_{IN} = I_0 + I_0 \cdot \sum_{k=0}^N 2^k \bar{b}_k \quad (2)$$

Where k= 0,1...N-1 is the bit number, I₀ is the current through Msc and the second term is the total current through the control transistors that are on varying in a binary fashion.

III. DCO

A. Introduction

The DCO is the combination of a digital-to-analog converter (DAC) and a voltage controlled oscillator (VCO). Based on the input code, the DAC converts the code to the voltage V_C. Then the voltage V_C controls the frequency of the VCO. Seen from Figure 6(a), the ring-type VCO can generate five clocks which are named as clk0-clk4, respectively. From Figure 6(b), it is seen that the delay cell consists of a modified NOR cell and two inverter cells. In order to reduce power, the signal Run turns to be high level when the PLL is not in use. Then the output of the delay cell keeps low level. When the signal Run is low level, the

voltage V_C controls the frequency of the VCO. The current M0 through increases as the voltage V_C increases, so the delay time of the delay cell decreases and the frequency of the VCO increases (or vice versa). Figure 6(c) shows that the voltage V_C is generated by the digital current controller. The PMOS transistors are (M8~M13) coded in a binary fashion, for example, the W/L ratio of M9 is twice that of M8 and so on. So, the range of the codes in the DCO is from 0 to 315. In order to obtain the minimum frequency of the DCO, M14 always keeps on the DCO, M14 always keeps on. The sizes of M15 and M16 are the same. M15 and M16 can act as resistors. So the voltage V_C increases with the increase of the current I_C.

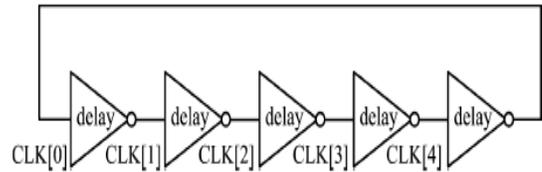


Figure 6(a) Structure of DCO

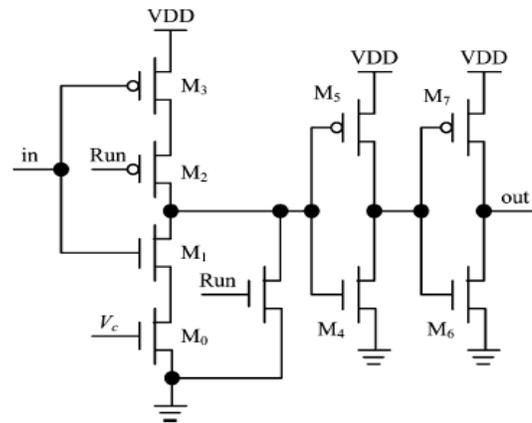


Figure 6(b) The circuit of the delay cell

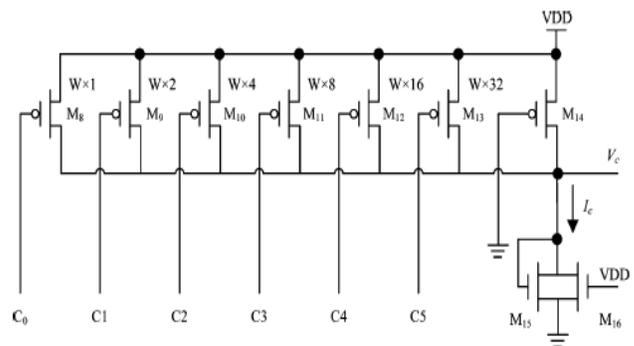


Figure 6(c) Digital Current Controller

B. Conventional DCO

The conventional DCO has three stages of driving strength controlled inverter cells and one AND gate for shutting down the DCO during idle mode. Like VCOs or CCOs, DCOs also have frequency controlled mechanism to control the output frequency of oscillation by means of digital control word applied at the control input of DCO. A variable delay inverter is a core element

of DCO and its precision directly affects the overall performance of DCO. The propagation delay time of inverter is inversely proportional to equivalent MOS width. With change in digital control word the equivalent width of MOS transistors varies, which changes the propagation delay time of the inverter.

With fixed supply voltage, two parameters modulate the output frequency of oscillator. One is total number of delay cells connected in the closed loop and other is propagation delay time of each delay cell. Block diagram of conventional DCO is shown in Figure 7. It employs the coarse code as well as fine code to control the output frequency. The circuit consists of three stages of driving strength controlled inverter cells and one AND gate to enable/disable the DCO. The W/L ratio of MOS transistors are binary weighted which enables to achieve binary incremental delays. The control bit applied at the input of first two stages is used for coarse tuning while the code applied at the control input of third stage provides fine tuning.

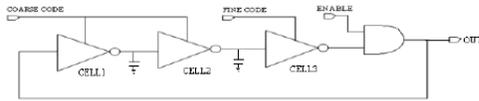


Figure 7 Conventional DCO

C. Proposed DCO

In proposed DCO-I structure, one driving strength controlled inverter cells & two NAND gates have been used as shown in Figure 8(a) and 8(b). In the second design, inverter cell & two NOR gates have been utilized as compared to three delay cell and one AND gate in conventional DCO.

In conventional DCO, control word is applied at the binary controlled input of all the three stages but in proposed DCO designs control word is applied only at the control input of first stage. Therefore, the propagation delay time of first stage i.e. driving strength controlled delay cell is only varied to control the output frequency of oscillation while propagation delay time of NAND/NOR gates remains fixed. As the number of transistors used in two proposed designs are much less than the conventional so circuit shows considerable power saving. The conventional DCO uses total 54 MOS transistors and two capacitors. On the other hand both modified circuits use only 24 MOS transistors. Due to less numbers of transistors delay time introduced by the circuit reduces and output operating frequency increases. However the numbers of frequency components that can be generated by proposed DCO are less than the conventional structure. There are applications which require particular specified frequency or need only a few frequency components. For those applications the proposed circuit shows power saving up to 40%.

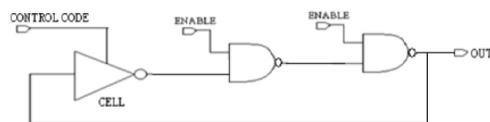


Figure 8(a) Proposed DCO-I

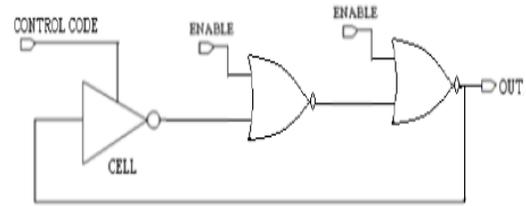
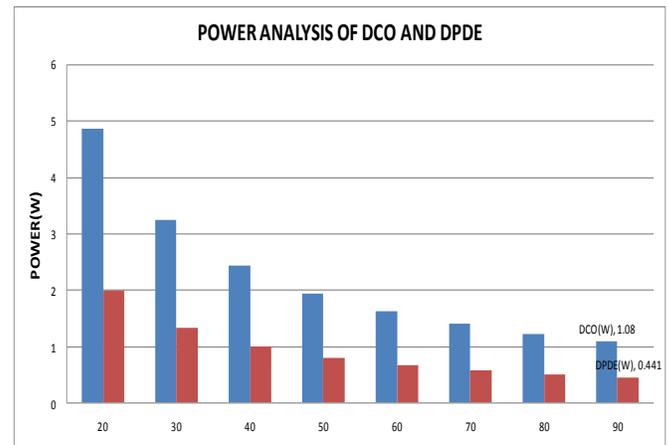


Figure 8(b) Proposed DCO-II

B. Simulation Results

The proposed DPDE was implemented in a standard 0.18μm process and transistor level simulation was carried out to verify the effectiveness of the methods. In order to eliminate the direct current paths in M3 and M4, the gate control voltage of M3 is delayed so that the two transistors are never on simultaneously. As can be seen M3 completely turns off before M4 turns on and M4 turns off before M3 turns on. The design procedure for this delay element is similar to the one presented.

The proposed DCOs and conventional DCO have been simulated and compared using TSPICE in 0.18μm (micrometer) technology. The two proposed DCO structures show significant increase in operating frequency with reduced power consumption.



IV. CONCLUSION

A Digitally Programmable Delay Element (DPDE) with very low power consumption has been presented. The proposed circuit is compared with two other architectures. By using a current mirror with feedback, the static current is eliminated and the dynamic power is made proportional to the delay with a maximum of 25μW power consumption. It is shown that the delay element will be more linear when implemented in improved technologies. The two new designs of DCO have been presented. The proposed method results in reduced power consumption than the conventional DCO and also reduces number of transistors. Finally DPDE and DCO are compared on the basis of their output power. By using improved CMOS technologies, power dissipation can be further reduced using delay element. The low power DPDE can also be used to implement many applications

such as DDPLs, ADPLLs, memory circuits, microprocessors and clock multipliers. There are applications which require particular specified frequency or need only a few frequency components. For those applications the proposed DCO circuit results in reduced power consumption.

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Authors

First Author – S.Jayasudha, Assistant Professor, P.A. College of Engineering and Technology and sudha.jayaudt@gmail.com.

Second Author – B.Ganga Devi, Assistant Professor, P.A. College of Engineering and Technology and deviikb@gmail.com