A Novel Low Power Optimization for On-Chip Interconnection

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Abstract- This paper presents a low power design methodology for the Quasi Resonant Interconnection networks (QRN). This focuses mainly on reducing the power utilized at the receiver by replacing the existing delay element by a digitally controlled delay element. The analysis and design of the transmitter, receiver and the Interconnect and spiral inductor models are presented using 0.18µm CMOS technology. A very efficient reduction in power can be obtained by this method as about 0.12W is the power at the proposed receiver when compared to 50W in the existing receiver.

Index Terms-Quasi resonant interconnection networks, delay element, spiral inductor,RZ-ASK modulation

I. INTRODUCTION

In various circuit modules transmitting signals over large areas required long interconnections.With the continuous scaling of technology and increased die area, cross sectional areas of wires has been scaled down while interconnect length & frequency has increased.

In [1] the damping factor and the ratio of the rise time of the input signal at the driver of an interconnect line to the time of flight of signals across the line are the two figure of merits that were studiedand a primary result of this study is that a range for the length of the interconnect exists for which inductance effects are prominent and under certain conditions, the inductance effects are negligible.

To overcome the above undesirable effects, many techniques developed over these years. Repeaters are often used [2] to minimize the delay required to propagate a signal through those interconnect lines that are best modeled as an RC impedance. But the major drawback was increased power dissipation and delay when used in large numbers when required. In [3] a current sensing method for ULV Applications is presented using a new auto-regulated current sensing scheme (ARCS).

In [4] it is shown that high performance can be obtained by using differential signaling, current mode sensing, bridge termination, and driver pre-emphasis. The adaptive bandwidth bus architecture based on hybrid voltage/current mode repeaters [5] for long global interconnect achieves high-data rates while minimizing static power dissipation. Low voltage signaling can also be used over long on-chip interconnects [6] [7].

A design which takes advantage of the inductance-dominated high-frequency regime of on-chip interconnects is shown capable of transmitting data at velocities near the speed of light [8]. This approach offers a five times improvement in delay over a conventional repeater insertion strategy but poor spectral efficiency. Alternatively a method was proposed [9] in which sharp current pulse data transmission was used to modulate transmitter energy to higher frequencies which provides considerably reduced dispersion.

It was found that the optoelectronic interconnects outperform their electrical counterparts, under certain conditions, especially for relatively long lines and multichannel data links [10]. But the major issue in this method is the interface between electrical and optical signals.

Finally, a low power, low latency on-chip interconnect design methodology based on inserting an on-chip spiral inductor to resonate interconnect around the fundamental harmonic of the transmitted signal was proposed. Thus, the interconnect capacitance resonates with the inserted on-chip inductance and the fundamental harmonic of the input signal is amplified and transmitted to the output. The energy resonates between electric and magnetic field rather than being dissipated as heat.

II. PRINCIPLE OF QUASI-RESONANT INTERCONNECTION

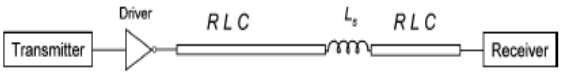


Figure 1: Quasi-resonant network

The quasi resonant interconnect network architecture is as shown above. The block consists of the transmitter, driver, and the RLC distributed interconnection or transmission line, on-chip spiral inductor L_s and a receiver.

The transmitter is used to modulate the input data signal for transmission. The inverter is used as a driver which drives the interconnect. The RLC transmission lines are found to be separated by the inductor Lswhich is used to resonate the

network at the desired frequency for minimum power consumption and delay. Finally the receiver demodulates the received modulated signal to the original input bit stream of data.

The fundamental harmonic of the input signal is amplified by the magnitude of the transfer function. Thus the network resonates at specific target frequency and magnitude. The output signal in the frequency domain is given by

$$V_{out}(s) = H'(s) \, . \, V_{in}(s) \quad (1)$$

$H'(s)$ is the transfer function of the network between and $V_{in}(s)$ is the

input data stream. The input data signal in the time domain can be given as,

$$v_{in}(t) = \sum_{k=-\infty}^{\infty} ake^{jk\omega pt} \quad (2)$$

where a_k is the k[th] harmonic of the signal and ω_p is the resonant radian frequency.

The average power consumed by the network is

$$P_{total,avg} = P_{trx,avg} + P_{qrn,avg} + P_{rec,avg} \quad (3)$$

where $P_{trx,avg}$ and $P_{rec,avg}$ are the average power consumption of the transmitter and receiver, respectively, and $P_{qrn,avg}$ is the average power consumption of the quasi-resonant network (including the driver). The resonant interconnect network is a passive linear network $P_{qrn,avg}$. A one-port network, as depicted in Fig. 8, can therefore be used to determine. The output impedance of the driver Rd and the input impedance of the network Zin determine the power consumption of the network.

III. OVERVIEW OF SPIRAL INDUCTOR MODEL

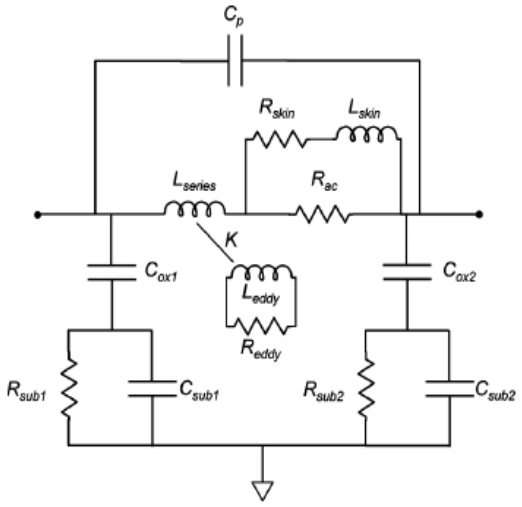


Figure 2: Lumped model of a spiral inductor

Figure 2 shows the lumped spiral inductor model. The capacitance C_p represents the capacitive coupling between the windings of the spiral inductor. The elements L_{series} and R_{ac} represent the inductance and parasitic resistance, respectively, while R_{skin} and L_{skin} model the skin effect. Also note that L_{series} incorporates the eddy current effect coupled to the inductor by the coefficient K. The parasitic capacitance between the lines and the substrate is modeled by C_{ox} . The parallel C_{sub} and R_{sub}combination models the parasitic resistance and capacitance to the substrate.

IV. DESIGN METHODOLOGY

This part contains the design of transmitter and receiver sections.

A. Transmitter Design

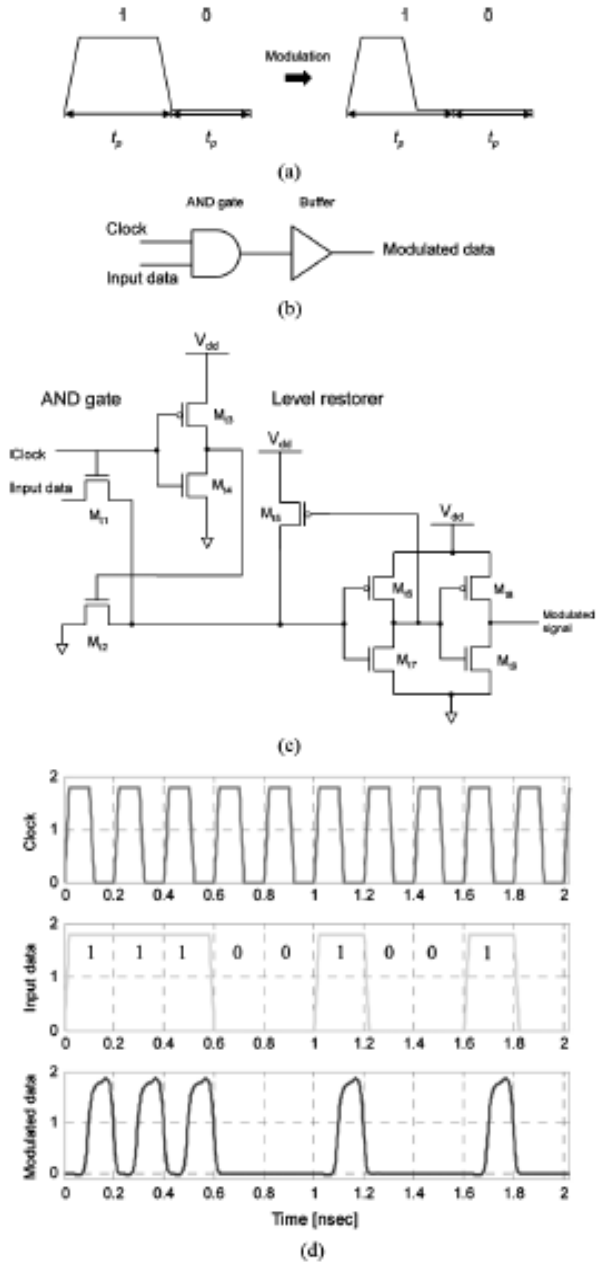


Figure 3: Transmitter circuit: (a) modulation scheme (b) gate level circuit (c) transistor level circuit (d) signal waveforms

The transmitter performs RZ-ASK (return to zero-amplitude shift keying) modulation inorder to support the single transmission frequency of $1/t_p$ bits/s. This method has three main advantages.

They are,

1. The transmitted signal has a single frequency.
2. Power is dissipated only during the half cycle period of transmission of logic 1.
3. No complex circuit is required.

The proposed modulation scheme and signal waveforms are shown in Fig. 3. To maintain high speed operation, a transmission gate-based circuit (consisting of transistors M_{t1}, M_{t2} , M_{t3} , and M_{t4}) is used for the logic, as shown in Fig. 3(c). In the case where both the clock and data are at logic one, the transmission gate M_{t1} passes the logic one state to the input of the buffer chain, while the inverter (consisting of transistors M_{t3} and M_{t4}) turns off transmission gate M_{t2}. In all of the other cases, the logic zero state is passed to the input of the buffer chain.

Transistor M_{t5} restores the voltage (equal to V_{th}) associated with the operation of transmission gates M_{t1} and M_{t2} . The input data as well as the modulated signal are shown in Fig. 5(d). In this example, a "100100111" bit stream is modulated at a 5-GHz operating frequency. Note that the modulated signal follows the return to zero amplitude shift keying scheme, essential for quasiresonant operation.

B.Receiver Design

The receiver circuit, its timing diagram and the signal waveforms are as shown in Fig. 4. When the clock is high, the switch closes and the data is sampled and transferred. The sampled signal charges (and discharges) the parasitic capacitance C_p . When the clock is low, the switch is open and the logic state is stored (or held) until the following clock cycle.

When the clock state is high, transistor M_{r1} turns on and the data is sampled and transferred. When the data state is low, the restorer transistor M_{r2} turns on, maintaining the high state signal at the input of the second inverter (consisting of transistors M_{r3} and M_{r4}). This mechanism serves a dual purpose. It restores the voltage associated with the transmission gate M_{r1} , and prevents charge leakage by replenishing the charge on the parasitic capacitance of transistors M_{r3} and M_{r4} (through the feedback connection).

When the clock logic is low, M_{r2} prevents the charge from leaking. When the data logic is high, transistor M_{r2} turns off and the logic low state is transferred to the output. Finally, when the clock state is low, the previous logic state is preserved until the following clock cycle.

Note that for the receiver to operate properly, the allowed skew between the clock and the incoming modulated data should be less then one quarter of the clock cycle. This constraint is required since the demodulation circuit is level sensitive. To synchronize the clock with the data, a delay element is used. A delay element based on inverters is used as shown in Fig. 4(c). The delay element provides a course and a fine delay. If course tuning is required (i.e., the delay of a half clock cycle,$t_p/2$), an odd number of inverters is used. If fine tuning is required (i.e., the intrinsic delay of the inverters), an even number of inverters is required. In this manner, for an odd number of inverters, a totaldelay of $t_p/2+n\delta$ is achieved. For an even number of inverters, a total delay of $n\delta$ is achieved. δ and n are the intrinsic delay of a single inverter and number of inverters, respectively.

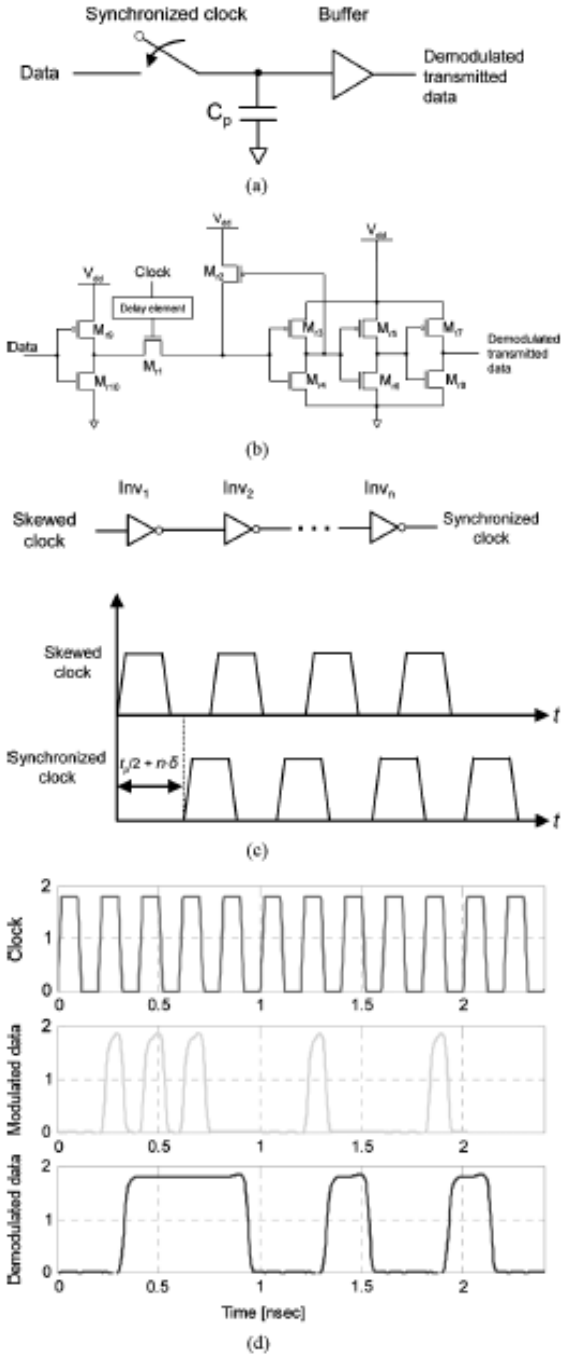


Figure 4: Receiver circuit: (a) sample and hold circuit (b) transistor level circuit (c) existing delay element circuit and timing diagram (d) signal waveforms.

V PROPOSED DELAY ELEMENT

The proposed delay element is as shown in Fig.5. In digitally controlled delay element by applying a specific binary vector to the controlling transistors (M_{n0} , $M_{n1,}$ …. $M_{p0,}$ $M_{p1,}$….), a combination of transistors are turned on at the sources of the M1 and M2 transistors. Such an arrangement, controls the rise and fall times (and hence, the delay) of the output voltage of the first inverter. The W/L ratios of the controlling transistors are usually chosen in a binary fashion so as to achieve binary, incremental delay.

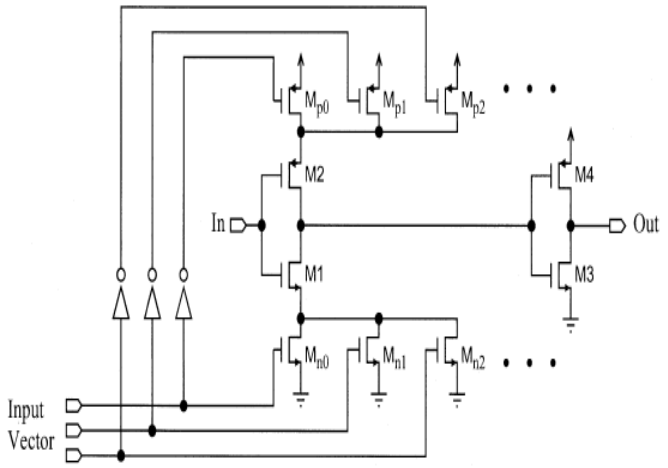


Figure 5: Digitally Controlled Delay Element

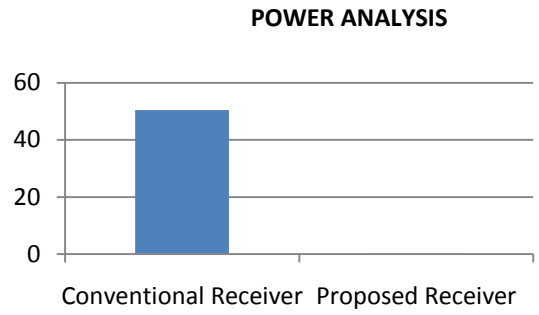
VI SIMULATION RESULT

The proposed delay element was implemented in a standard 0.18µm process and transistor level simulation was carried out to verify the effectiveness of the methods. Table 1 summarizes the performance of the presented delay element in the receiver with the one reported. The power is only0.1289W in the proposed receiver when compared to 50.43W in the conventional receiver.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

Receiver Type	Conventional Receiver	Proposed Receiver
Power(W)	50.43W	0.1289W

The proposed receiver and conventional receiver have been simulated and compared using TSPICE in 0.18µm (micrometer) technology. The two proposed receiver structures show significant decrease in power consumption.



VII CONCLUSION

Thus the receiver using the proposed digitally controlled delay element has been presented. The method is based on 0.18µm CMOS technology. An accurate model is presented based on transmission line theory and a lumped high frequency model of an on-chip spiral inductor. This method is shown to outperform the conventional method. The receiver power value using conventional method is 50.43W whereas the power value of the proposed receiver is 0.1289W.Thus significant power reduction is achieved.

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