# Low Complexity and High Accuracy Fixed Width Modified Booth Multiplier

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***Abstract-*** In many high speed Digital Signal Processing (DSP) and multimedia applications, the multiplier plays a very important role because it dominates the chip power consumption and operation speed. In DSP applications, in order to avoid infinite growth of multiplication bit width, it is necessary to reduce the number of multiplication products. Cutting off n-bit Less Significant Bit (LSB) output can construct a fixed width multiplier with n-bit input and n-bit output. However, truncating the LSB part leads to a large number of truncation errors. In order to avoid truncation error, error compensation circuit is designed with less truncation error and less hardware over head. A new error compensation circuit by using the dual group minor input correction vector to lower input correction vector compensation error is proposed. As compared with the conventional multiplier, the proposed fixed width modified booth multiplier performs not only with lower compensation error but also with lower hardware complexity, especially as multiplier input bits increase. In the proposed fixed width multiplier, the truncation error can be lowered compared with the direct truncated multiplier and the transistor count can be reduced compared with the full length multiplier.

***Index Terms-*** Fixed Width Multiplier, Modified Booth Multiplier, Error Compensation Circuit, Partial product Generator, CSA Tree.

## I. INTRODUCTION

Multiplier plays an important role in today's digital signal processing and various other applications. With advances in technology, many researchers have tried and are trying to design multipliers which offer either of the following design targets high speed, low power consumption, regularity of layout and hence less area or even combination of them in one multiplier thus making them suitable for various high speed, low power and compact VLSI implementation. Multiplication involves two basic operations, the generation of partial products and their accumulation. The former operation is generally implemented by AND gates and the latter is implemented by several CSA stages. Basically each CSA stage consists of n CSA cells that take three inputs of the same weight and generates two outputs. Each CSA stage sums up one additional partial product, and the intermediate partial product is kept in so called carry save form. As there is no carry propagation in a CSA stage, the total delay is independent of the number of bits of a partial product but depends on the number of partial products. Therefore, an important objective in the design of a multiplier is to reduce the number of partial products. The most popular partial product recoding scheme is known as the modified Booth recoding.

In this paper, an enhanced error compensation design for fixed width modified booth multiplier is proposed. The proposed modified booth multiplier consists of partial product generator, CSA Tree and the circuit is simplified using De Morgan's law. A new error compensation circuit by using the dual group Minor Input Correction (MIC) vector to lower Input Correction(IC) vector compensation error is designed. By the symmetric property of MIC, fan-in can be reduced to half and hardware in up-MIC and down-MIC can be shared. Then, the hardware complexity of circuit is lowered. De Morgan's simplification is performed to decrease the transistor count of the compensation circuit [1]. In [2] a high-accuracy error compensation circuit for the fixed-width modified Booth multiplier is proposed. To reduce the truncation error, the partial product matrix of Booth multiplication is modified and an effective error compensation function is derived that makes the error distribution be more symmetric to and centralized in the error equal to zero, leading the fixed width modified Booth multiplier to very small mean and mean-square errors. In addition, a simple compensation circuit mainly composed of the simplified sorting network is also proposed. Compared to the previous circuits, the proposed error compensation circuit can achieve a tiny mean error and a significant reduction in mean-square error. In [6] Truncated multipliers compute the most-significant bits of the n x n bits product. This paper focuses on variable-correction truncated multipliers, where some partial-products are discarded, To reduce complexity, and a suitable compensation function is added to partly compensate the introduced error. The optimal compensation function, that minimizes the mean square error, is obtained in this paper in closed form.

## II. FUNDAMENTAL OF MODIFIED BOOTH MULTIPLIER

Let us consider the multiplication operation of two n –bit signed numbers A=an-1 a n-2…..a0 (multiplicand) and B=bn-1 b n-2…..b0 (multiplier). The two's complement representations of A and B can be expressed as follows:

$$A = -a_{n-1}2^{n-1} + \sum_{i=0}^{n-2} a_i 2^i, \quad B = -b_{n-1}2^{n-1} + \sum_{i=0}^{n-2} b_i 2^i. \tag{1}$$

By modified Booth encoding which groups the bits of the multiplier into triplets, can be expressed as,

$$B = \sum_{i=0}^{n/2-1} M_i 2^{2i} = \sum_{i=0}^{n/2-1} (-2b_{2i+1} + b_{2i} + b_{2i-1}) 2^{2i} \quad (2)$$

The Modified Booth Encoding Table is follows as

**Table I - Modified Booth Encoding Table**

| $b_{2i+1}$ | $b_{2i}$ | $b_{2i-1}$ | Operation | $neg_i$ | $two_i$ | $one_i$ | $zero_i$ | $cor_i$ |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | +0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | +A | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | +A | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | +2A | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 0 | -2A | 1 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | -A | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | -A | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | -0 | 1 | 0 | 0 | 1 | 0 |

## III. PROPOSED FIXED WIDTH MODIFIED BOOTH MULTIPLIER

The proposed width modified booth multiplier consists of partial product generation circuit. It generates the partial products when the multiplication is performed. Then CSA Tree and De Morgan's circuit is present.

### A. PARTIAL PRODUCT GENERATION CIRCUIT:

If the Multiplicand and multiplier are of n-bits then the partial product generator generates (0……..n/2-1) n/2 number of one dimensional partial product bits.Figure1 shows the partial product generation diagram.

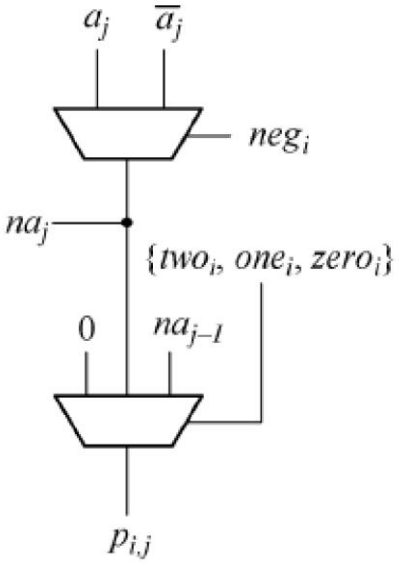


**Figure 1: Partial Product Generation Circuit**

### B.CSA TREE

A Carry Save Adder is just a set of one bit full adders, without any carry chaining. Therefore, an n-bit CSA receives three n-bit operands, namely A(n-1)..A(0), B(n-1)..B(0), and CIN(n-1)..CIN(0), and generates two n-bit result values, SUM(n-1)..SUM(0) and COUT(n-1)..COUT(0).

The most important application of a carry save adder is to calculate the partial products in integer multiplication. This allows for architectures, where a tree of carry save adders (so called *Wallace tree*) is used to calculate the partial products very fast. One 'normal' adder is then used to add the last set of carry bits to the last partial products to give the final multiplication result. Usually, a very fast carry look ahead or carry select adder is used for this last stage, in order to obtain the optimal performance.

There are many cases where it is desired to add more than two numbers together. The straightforward way of adding together m numbers (all n bits wide) is to add the first two, then add that sum to the next, and so on. This requires a total of m − 1 additions, for a total gate delay of O(mlg n) (assuming lookahead carry adders). Instead, a tree of adders can be formed, taking only O(lgm · lg n) gate delays. Using carry save addition, the delay can be reduced further still. The idea is to take 3 numbers that have to add together, x + y + z, and convert it into 2 numbers c + s such that x + y + z = c + s, and do this in O(1) time. The reason why addition cannot be performed in O(1) time is because the carry information must be propagated. In carry save addition, refrain from directly passing on the carry information until the very last step. Illustration of the general concept with a base 10 example as follows:

To add three numbers by hand, typically align the three operands, and then proceed column by column in the same fashion that have perform addition with two numbers. The three digits in a row are added, and any overflow goes into the next column. Observe that when there is some non zero carry, then really adding four digits (the digits of x,y and z, plus the carry).

The carry in signal is considered as an input of the CSA, and the carry out signal is considered as an output of the CSA. The computation can be divided into two steps, first compute S and C using a CSA, then use a CPA to compute the total sum. From this example, the carry signal and the sum signal can be computed independently to get only two n-bits numbers has been observed. A CPA is used for the last step computation and the carry propagation exist only in the last step.

### C. DEMORGAN'S LAW

In propositional logic and Boolean algebra, De Morgan's laws are a pair of transformation rules that are both valid rules of inference. The rules allow the expression of conjunctions and disjunctions purely in terms of each other via negation. De Morgan's laws are used to simplify Boolean equations so that equations can be build only involving one sort of gate, generally only using NAND or NOR gates. This can lead to cheaper hardware.

In set theory, de Morgan's laws relate the three basic set operations to each other; the union, the intersection, and the complement.

If A and B are subsets of a set X , de Morgan's laws state that

(A B) (A B) = A B A B

Here, denotes the union, denotes the intersection, and A denotes the set complement of A in X.

Above, de Morgan's laws are written for two sets. In this form, they are intuitively quite clear. For instance, the first claim states that an element that is not in A B is not in A and not in B . It also states that an elements not in A and not in B is not in A B. In extensions of classical propositional logic, the duality still holds (that is, to any logical operator that can always find its dual), since in the presence of the identities governing negation, one may always introduce an operator that is the De Morgan dual of another. This leads to an important property of logics based on classical logic, namely the existence of negation normal forms: any formula is equivalent to another formula where negations only occur applied to the non logical atoms of the formula. The existence of negation normal forms drives many applications, for example in digital circuit design, where it is used to manipulate the types of logic gates, and in formal logic, where it is a prerequisite for finding the conjunctive normal form and disjunctive normal form of a formula. Computer programmers use them to simplify or properly negate complicated logical conditions. They are also often useful in computations in elementary probability theory.

## IV. .EXPERIMENTAL RESULTS

The experimental result shows us the Error comparison of Normal Conventional Multiplier and Proposed Multiplier is shown in the table2.

**Table 2: Comparison of Normal Conventional Multiplier and Proposed Multiplier**

| INPUTS | | NORMAL | PROPOSED | ERROR VALUE | | REDUCED ERROR |
|---|---|---|---|---|---|---|
| X | Y | MULTIPLIER | MULTIPLIER | DIRECT | PROPOSED | |
| 101010 | 101010 | 011011 | 011100 | 36 | 28 | 8 |
| 110101 | 110101 | 101011 | 101100 | 57 | 7 | 50 |
| 110101 | 101010 | 100010 | 100011 | 50 | 14 | 36 |
| 111111 | 111111 | 111110 | 111110 | 1 | 1 | 0 |
| 011001 | 110111 | 010101 | 010110 | 31 | 33 | 2 |
| | | | AVERAGE | 35 | 16.6 | 18.4 |

## V. CONCLUSION

In this proposed fixed width modified booth multiplier, a new error compensation circuit is designed and there is less truncation error. In this approach the partial products are reduced and it results in lower hardware complexity and less partial products.

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