ISSN 2250-3153

Design and Implementation of 8X8 Truncated Multiplier on FPGA

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Abstract- Multiplication is frequently required in digital signal processing. Parallel multipliers provide a high-speed method for multiplication, but require large area for VLSI implementations. In most signal processing applications, a rounded product is desired to avoid growth in word size. Thus an important design goal is to reduce the area requirement of the rounded output multiplier. This paper presents a method for parallel multiplication which computes the products of two n-bit numbers by summing only the most significant columns with a variable correction method. This paper also presents a comparative study of Field Programmable Gate Array (FPGA) implementation of 8X8 standard and truncated multipliers using Very High Speed Integrated Circuit Hardware Description Language (VHDL). Truncated multipliers can be used in finite impulse response (FIR) and discrete cosine transforms (DCT). The truncated multiplier shows much more reduction in device utilization as compared to standard multiplier. Significant reduction in FPGA resources, delay, and power can be achieved using truncated multipliers instead of standard parallel multipliers when the full precision of the standard multiplier is not required.

Index Terms- Digital Signal Processing (DSP), Field Programmable Gate Array (FPGA), Truncated Multiplier, Variable correction method, VHDL

I. INTRODUCTION

Parallel multipliers provide high speed method for multiplications, but require large area for VLSI implementation. In most signal processing applications, rounded product is required to avoid growth in word size. Thus an important aim is to design a multiplier which required less area and that is possible with the truncated multiplier. In the wireless multimedia word, DSP systems are ubiquitous. DSP algorithms are computationally intensive and test the limits of battery life in portable device such as cell phones, hearing aids, MP3 players, digital video recorders and so on. Multiplication is the main operation in many signal processing algorithms hence efficient parallel multipliers is desirable. A full-width digital n × n bits multiplier computes the 2n bits output as a weighted sum of partial products. A multiplier with the output represented on n bits output is useful, as example, in DSP data paths which saves the output in the same n bits registers of the input. A truncated multiplier is an n × n multiplier with n bits output. Since in a truncated multiplier the n less significant bits of the full-width product are discarded, some of the partial products are removed and replaced by a suitable compensation function, to trade-off accuracy with hardware cost. As more columns are eliminated, the area and power consumption of the arithmetic unit are significantly reduced, and in many cases the delay also decreases.

The trade-off is that truncating the multiplier matrix introduces additional error into the computation. Recent advancements in VLSI technology and in particular, the increasing complexity and capacity of state-of-the-art programmable logic devices have been making hardware emulations possible. The underlying key of the emulation system is to use SRAM-based field programmable gate arrays (FPGAs) which are very flexible and dynamically reconfigurable. In many cases implementation of DSP algorithm demands using Application Specific Integrated Circuits(ASICs).The development cost for Application Specific Integrated Circuits(ASICs) are high, algorithms should be verified and optimized before implementation. The Digital Signal Processing (DSP), image processing and multimedia requires extensive use of multiplication. The truncated multipliers can easily be implemented using Field Programmable Gate Array (FPGA) devices.

In FPGAs, the choice of the optimum multiplier involves three key factors: area, propagation delay and reconfiguration time. An FPGA is a digital integrated circuit that comes in a wide variety of size and with many different combinations of internal and external features. The state-of-the-art FPGAs consist of relatively small blocks of programmable logic. These blocks, each of which typically contains a few registers and a few dozen low level, configurable logic elements, are arranged in a grid pattern and tied together using programmable interconnects. The truncated multipliers can be designed using either constant correction method or variable correction method.

CONSTANT CORRECTION METHOD

In constant correction method design the lower N columns of a parallel multiplier are truncated and a correction is then added to the remaining most significant columns. The Constant Correction Methods (CCM) uses a constant value, independent on the actual values of the inputs, in order to estimate the LSP minor.

The multiplier output can be written as:

PCCM = truncn(SMSP + SLSP major + constant) -------- (1)

where SLSP major is the weighted sum of the elements of the LSP major.

In this technique the LSP is eliminated and is substituted by a constant term, calculated considering only the lose carries. This approach reduces up to 50% the area of the full-width multiplier, but introduces a rather large error, which rapidly increases with n, resulting impractical in most applications.

VARIABLE CORRECTION METHOD

The basic design of the multiplier is the same as that of a constant correction fixed width multiplier. The least significant N-2 partial product columns of a full width multiplier are truncated. The partial product terms in the N- 1
column are then added to the partial product terms in the N^{th} column using full-adders. This is done in order to offset the error introduced due to truncation of least significant N- 2columns. The correction term that is generated is based on the following arguments,

1) The biggest column in the entire partial product array of a full-width multiplier is the N^{th}column.

2) The N^{th} column contributes more information to the most significant N-1 columns than the rest of the least significant N-1 columns. The information presented could be made more accurate if the carry from the N- 1^{th} column is preserved and passed onto the N^{th} column.

3) Adding the elements in N- 1^{th} column to the N^{th} column provides a variable correction as the information presented is dependent on input bits. When all the partial product terms in the N-1^{th} column are zero, the correction added is zero. When all the terms are one, a different correction value is added.

The accuracy of truncated multipliers can be significantly improved using variable correction truncated multipliers that compensate the effect of the dropped terms with a non constant compensation function. The multiplier output is computed as:

PVCM = truncn (SMSP + SLSP major + f (IC) + Kround)--(2)
where f (IC) is a suitable compensation function.

The objective of this paper is to present a comparative study of variable truncated and standard multiplier by implementing the 8×8-bit respective multiplier using Spartan-3AN FPGA device. This paper is organized as follows. In section II, the mathematical basis of truncated multiplication is briefly discussed. Section III presents the FPGA design and implementation results and finally conclusion is provided in section IV.

II.MATHEMATICAL BASIS OFTRUNCATED MULTIPLIER

Considering the multiplication of two n-bit inputs A and B, a standard multiplier performs the following operations to obtain the 2n bit product P.

$$A = \sum_{i=1}^{n} a_i 2^{-i} \quad \text{--------- (3)}$$

$$B = \sum_{j=1}^{n} b_j 2^{-j} \quad \text{---------- (4)}$$

$$P = \sum_{i=1}^{2n} p_i 2^{-i} = \sum_{i=1}^{n}\sum_{j=1}^{n} A_i B_j 2^{-i-j} \quad \text{--- (5)}$$

where ai,bi and Pi represent the ith bit of A, B and P, respectively. The output of the 8x8 truncated multiplier can be written as below.

$$A = \sum_{i=1}^{n} a_i 2^{-i} \quad \text{--------- (6)}$$

$$B = \sum_{j=1}^{n} b_j 2^{-j} \quad \text{---------- (7)}$$

$$P = AB = \sum_{i=1}^{n} p_i 2^{-i} \quad \text{---------- (8)}$$

Fig.1 shows the block diagram of standard 8x8 multiplier. Fig. 2 shows the architecture of standard 8×8-bitparallel multiplier, where HA and FA are the half and full adders respectively.

III. FPGA DESIGN AND IMPLEMENTATION RESULTS

The design of standard and truncated 8×8 bit multipliers are done using VHDL and implemented in a Xilinx Spartan 3AN XC3S700AN (package: fgg484, speed grade: -5) FPGA using the Xilinx ISE 9.1i design tool. Fig. 1 shows the block diagram of standard multiplier. The internal RTL schematic of the standard 8x8 multipliers shown in fig.3.The behavioural simulation presents the utilization of MSB as the required value in truncated multiplier for example, $255x255=(65025)_{10}=(1111111000000001)_2=(11111110)_2 =(254)_{10}$ is obtained in the simulation result of truncated multiplier.

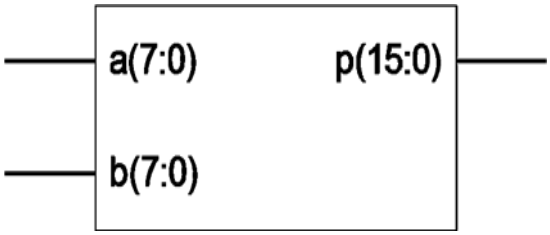

Fig.1 Block dig. of standard 8x8 multiplier

Fig.4 shows the block diagram of truncated 8x8 multiplier.Fig.5 shows the architecture of truncated 8x8 multiplier. The internal RTL schematic of truncated 8x8 multiplier is shown in fig.6.The total equivalent gate count in case of standard 8x8 multiplier is 702 and that is improved to 456 using truncated 8x8 multiplier. The power consumption incase of standard 8x8 multiplier is 419mW and that is also improved to 156mW using truncated 8x8 multiplier. The number of occupied slices used in truncated multiplier is also improved. In case of standard 8x8 multiplier it is 60 and in truncated 8x8 multiplier it is 42.

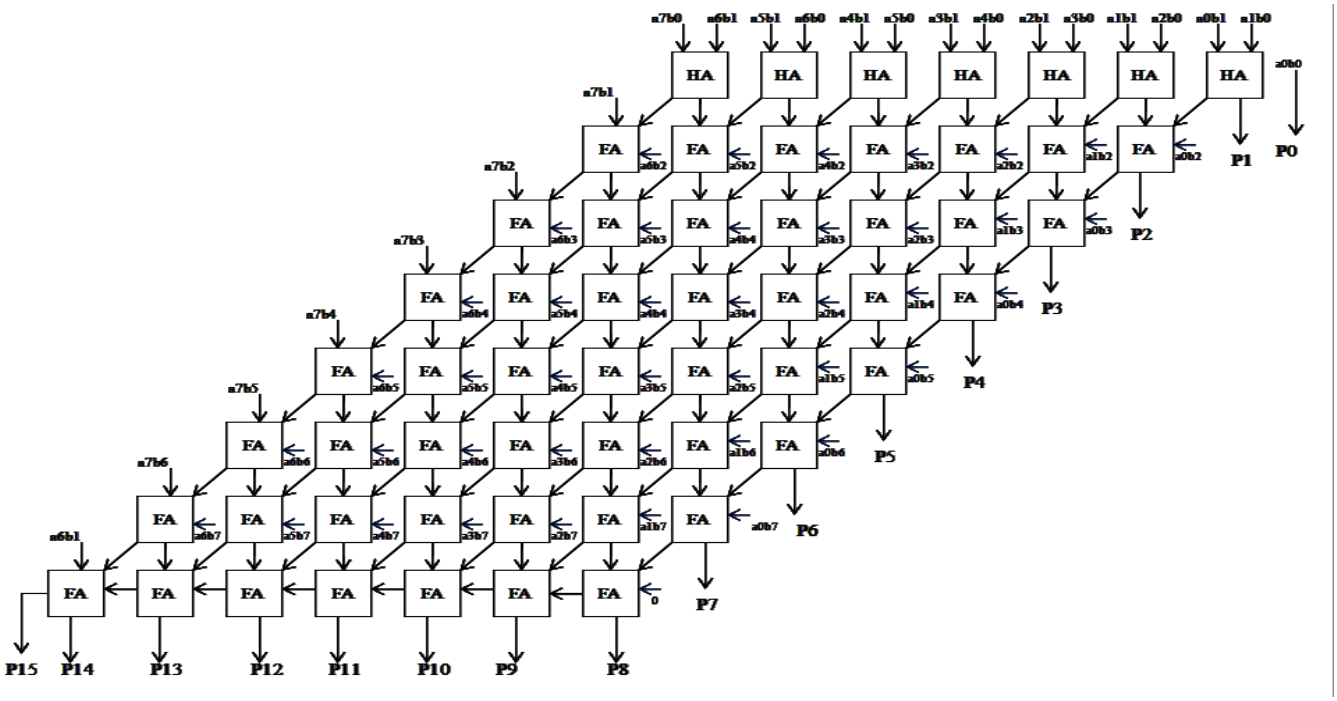

Fig.2 Architecture of 8x8 standard multiplier.

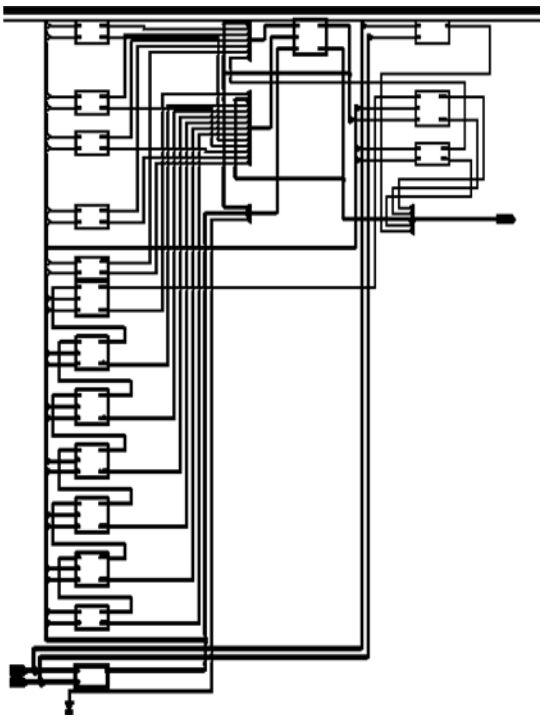

Fig.3 RTL schematic of standard 8x8 multiplier.

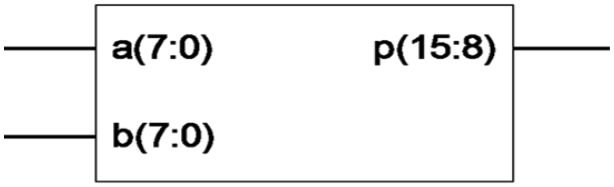

Fig.4 Block dig. of truncated 8x8 multiplier.

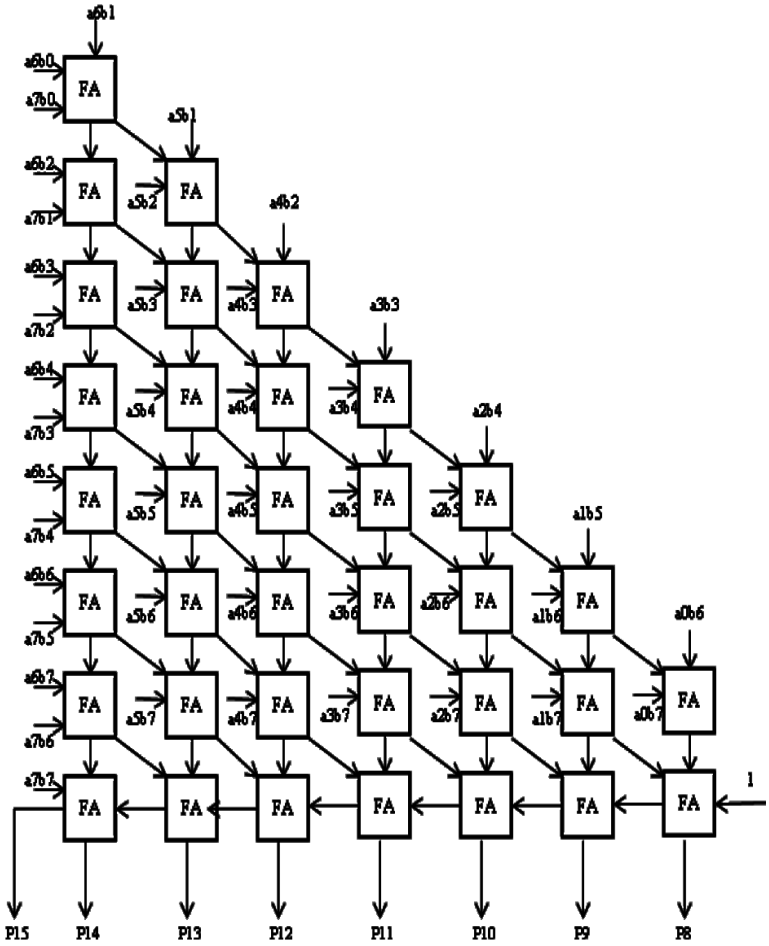

Fig.5 Architecture of truncated 8x8 multiplier.

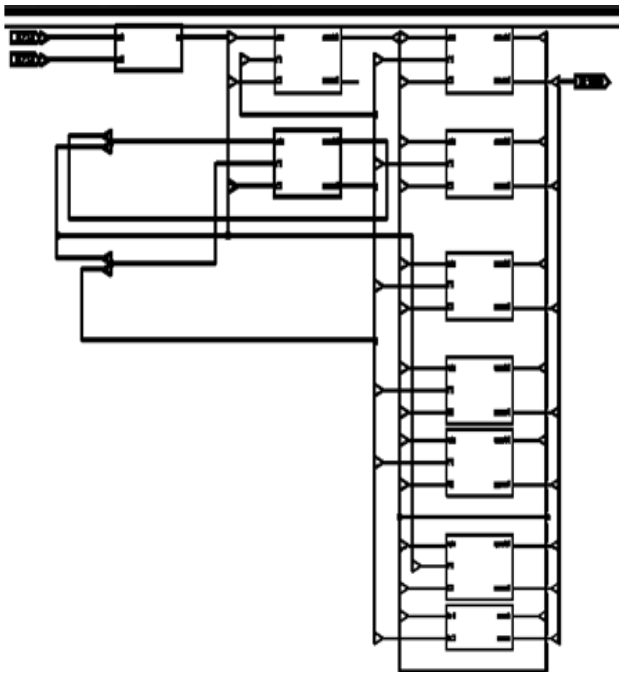

Fig.6 RTL Schematic of truncated 8x8 multiplier.

TABLE I

FPGA RESOURCE UTILIZATION FOR STANDARD AND TRUNCATED 8X8 MULTIPLIER

Device(SPARTAN 3AN) XC3S700ANFGG484-5		
	STANDARD	TRUNCATED
Total equivalent gate count	702	456
JTAG gate count for IOBs	1536	1152
Power(mW)	419	156
Four input LUTs	117/4704	76/4704
Number of occupied slices	60/2352	42/2352
Number of bonded IOBs	32/176	24/176

CONCLUSION

In this paper we have presented hardware design and implementation of FPGA based parallel architecture for standard and truncated 8x8 multipliers utilizing VHDL. Both the design were implemented on Xilinx Spartan 3AN XC3S700AN FPGA device. The aim is to present a comparative study of the standard and truncated 8x8 multipliers. The truncated multiplier as compared to standard multiplier shows much more reduction in device Utilization. The power consumption of standard 8x8 multiplier is 419mW and that to truncated 8x8 multiplier power consumption is only 156 mW. The truncated 8x8 multiplier uses only 42 slices out of 2352 slices. Truncated multiplication provides an efficient method for reducing the power dissipation and area of parallel multipliers.

ACKNOWLEDGMENT

The satisfaction that accompanies a successful completion of any task would be incomplete without the mention of people, whose constant guidance and encouragement crowned the efforts with success. I express my heartfelt thanks to my guide Ms. Sharda G.Mungle for providing me an opportunity and excellent environment to carry out my work under her..I would like to further extend my heartfelt thanks to the HOD Electronics engg.dept.KITS,Ramtek.

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SIMULATION RESULTS OF STANDARD AND TRUNCATED MULTIPLIERS