DESIGN OF HIGH SPEED AND LOW POWER 4T SRAM CELL

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Abstract: Portable devices demand for low power dissipation. To reduce power dissipation, the subsystem in a device needs to be designed to operate at low power and also consume low power. Significant progress has been made in low power design of dynamic RAM's. Static RAM's are also critical in most VLSI based system on chip applications. Basic SRAM bit cell consists of 6T. Few designs using 4T are also available in open literature. In this paper a highly reliable, low power and high speed SRAM design is proposed and comparisons were made with 6T and basic 4T SRAM designs.

Keywords: Power dissipation, Dynamic RAM, Static RAM, 6T-SRAM, 4T-SRAM.

I. INTRODUCTION

CMOS scaling has offered significant improvement in performance for the past four decades. However, as technology scaled down, standby power consumption was increased exponentially with the decrease of threshold voltage of MOSFET devices [1,2]. SRAM being one of the important sources of static power consumption demands its mere existence in most of the digital circuits. This challenge of optimizing the power consumption gives us the very need to design a new low power SRAM to enable the digital world set itself into miniature model.

II. CONVENTIONAL 4T SRAM CELL DESIGN

4T SRAM cell is the key SRAM component storing binary information. A typical SRAM cell uses two PMOS and two NMOS transistors forming a latch and access transistors. Access transistors enable access to the cell during read and write operations and provide cell isolation during the unaccessed state an SRAM cell is designed to provide non-destructive read access, write capability and data storage (or data retention) for as long as cell is powered[2,3]. The conventional 4T-SRAM consists of both nMOS and pMOS. In general, the cell design must strike a balance between cell area, robustness, speed, leakage and yield. Power reduction is one of the most important design objectives. However, power cannot be reduced indefinitely without compromising with other parameters like cell area and speed of operation. The mainstream four-transistor (4T) CMOS SRAM cell is shown in Figure-1, four transistors (q1−q4) comprise cross-coupled CMOS inverters and two nMOS transistors q2 and q4 provide read and write access to the cell.

A 6T CMOS SRAM cell is the most popular SRAM cell due to its superior robustness, low power and low-voltage operation. It is well known that the 4T-SRAM cells have dominated the standalone SRAM market since they occupy much less cell area than 6T-SRAM cells[2,3]. However, for on-chip storage in microprocessors and other logic circuits, the 4T-SRAMs have not been used, because they need a complex process to form a load element and have poor stability at low voltage.

The conventional 4T-SRAM cell design and layout is shown in Figures 1 and 2 respectively. It consists of two nMOSFETs and two pMOSFETSs for drive transistors and transfer gates, and two load elements to hold cell data. During READ/WRITE operation, a high-node level in the SRAM cell is lower than a supply voltage (V_{dd}) by a threshold voltage of the transfer transistor, even though both bit lines are precharged at V_{dd}. This is because transfer gates operate as source-follower circuits when the cell is selected[4]. After closing the transfer gate, current through the load element raises the high-node level to (V_{dd}) but it takes an order of milliseconds since the current is, in most cases, 1–10pA[1]. During this transient time as well as *READ/WRITE* operation itself, this 4T-SRAM cell is very unstable against noise from peripheral circuits because of less critical charge.

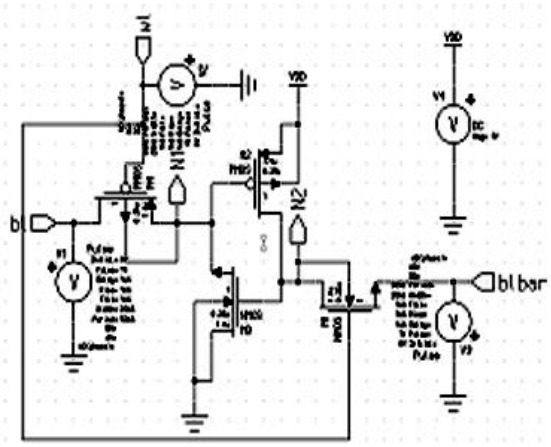

Figure 1. Conventional 4T SRAM cell

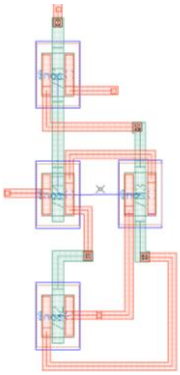

Figure 2. Layout of 4T SRAM

Although dynamic (switching) power is the dominant source of power dissipation, static (leakage) power is increasing exponentially and is projected to become severe over the next several technology generations, with some estimates as high as 50% or more of total power. The largest source of leakage power is in large array structures, of which caches and branch predictors are among the largest[5,6]. The risk of state-losing techniques is that premature deactivation may lose useful data, incurring a later induced cache miss. State-preserving techniques avoid this problem but have higher standby leakage currents.

Conventional SRAM design has the problem of large capacitive loads that must be switched when moving between active and standby mode. A new read circuit is proposed as an individual read operation will be performed and the bit lines are precharged to VDD[7,8]. The read operation is initiated by enabling the word line (WL) and connecting the precharged bit lines, BL and BLB, to the internal nodes of the cell. Upon read access, the bit line voltage VBL remains at the precharge level. The complementary bit line voltage VBLB is discharged through transistors Q1 and Q3 connected in series[8,9]. Effectively, transistors Q1 and Q3 form a voltage divider whose output is now no longer at zero volts and is connected to the input of inverter Q2−Q4. Sizing of Q1 and Q3 should ensure that inverter Q2−Q4 do not switch causing a destructive read.

4T cells are as fast as 6T cells, but they do not store charge indefinitely. Rather, the charge gradually leaks away at a rate that is a function of the cell's specific design as well as the current operating temperature[5,7]. This caps the amount of leakage energy that an unused cell can dissipate. Since power and ground lines need not stripe vertically down the array, 4T cells can have area benefits as well. 4T cells are especially applicable to on-chip structures whose data is both transient and predictive.

An attempt is made to address problems like charge leakage and large capacitive loads leading to delay and power dissipation in conventional 4T SRAM Cell design by proposing suitable modifications in the next section[6,8].

PROPOSED 4T SRAM

The proposed 4T SRAM cell with inverter is shown in figure 3 which improves the power and stability of write operation. These cells have no connection to Vdd and thus inherently provide decay functionality: values are refreshed upon access but discharge over time without use[8]. Much of on-chip storage is devoted to transient, often short lived data. Despite this, virtually all on-chip array structures use 4T static RAM cells that store data indefinitely. This makes 4T cells uniquely well-suited for predictive structures like branch predictors and BTBs where data integrity is not essential.

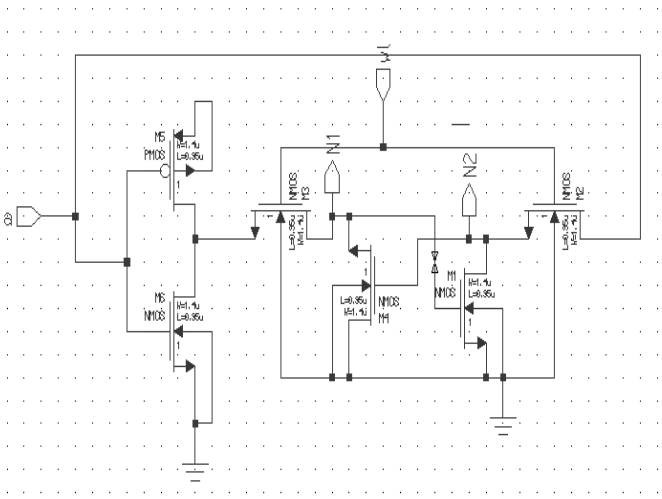

Figure 3. Proposed 4T SRAM cell using inverter

There are three premiere capacitances in SRAM cell. These capacitances include BL and BLB capacitances, word lines capacitances. BL and BLB capacitances are mainly composed drain junction capacitance of access transistor of SRAM cell. Next large capacitance in SRAM cell is word-lines capacitance and mainly composed of gate capacitance of access transistors of SRAM cell[9]. These capacitances mainly composed drain junction capacitance of access transistors of 4T SRAM cell and gate capacitances and drain junction capacitance of PMOS load transistors and NMOS drive transistors.

Locality is relevant in the SRAM design because it impacts how 4T cells are refreshed[7]. Branch predictors are typically laid out as a square, with each row having multiple neighboring predictors. In a squarified predictor, reading a row refreshes all the cells in a row because the WL is asserted. Retention time selection and locality granularity go together because large row granularity makes the apparent rate of refresh much higher. Cells that would have decayed if left alone get refreshed coincidentally by nearby active cells[4]. Thus 4T cells with short retention times may not lose data as quickly if the row size is long enough. In contrast, in a design with very fine row granularity one would opt for 4T cells with very long retention times.

Proposed 4T SRAM had been implemented and its write operation is observed with the inverter condition using one input source for both BL and BLBAR. When applying the input the BL and BLBAR will be in inverse and WL should raise either from 0 to 1 or from 1 to 0 for successful write operation.

RESULTS

Simulation of SRAM Cell is done using Mentor Graphics Tools using 130nm technology. The output waveforms of Conventional and Proposed 4T SRAM cells are shown in Figure 4 & 5. The reliability of SRAM cell depends on the power consumed by the circuit which is the main requirement for SRAMs in portable devices.

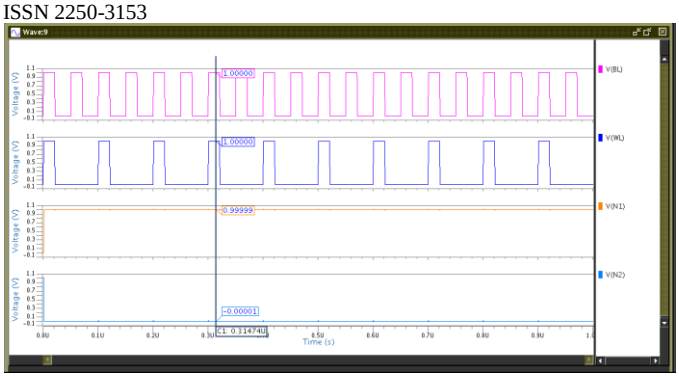

Figure 4: Waveforms of 4T Conventional SRAM

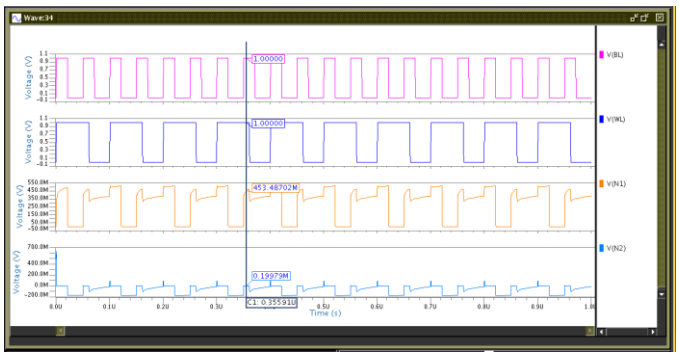

Figure 5: Waveforms of Proposed 4T SRAM

TABLE I. PERFORMANCE COMPARISON OF CONVENTIONAL & PROPOSED 4T-SRAM

Parameters	4TSRAM	Proposed 4TSRAM
Area	19.22µm²	26.92µm²
Delay	27.5ps	17.9ps
Static power disspation	75.24nw	44.85nw
Total power dissipation	667.6µw	459µw

CONCLUSION

The proposed 4T SRAM Cell is designed using nMOS transistors and an inverter to achieve high reliability and high density SRAM. The proposed SRAM cell static power dissipation is reduced by 41% and total power dissipation by 32 % , delay is reduced by 36% and occupies 32.46% less area when compared with conventional 6T SRAM and 26% more area compared with conventional 4T SRAM cell. As the Proposed Model dissipates less power and has reduced delay it is useful for the design of memories in power efficient applications.

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