A NML-HDL Snake Clock Based QCA Architecture

[1]Mr. M. B. Kachare, [2]Dr. P. H. Zope

[1]ME I[st] (Dig. Electronics), [2]Asst. Professor (E&TC Dept.), [1,2]SSBT's COET, Bambhori, Jalgaon
[1]mayur.kachare@rediffmail.com, [2]phzope@gmail.com

Abstract- The international technology roadmap of semiconductors suggests that quantum-dot cellular automata (QCA) technology might be possible CMOS substitute [4]. MQCA are attractive due to their compactness and extremely small power dissipation. This led to focus on nanomagnetic logic (NML). The nature of these circuits is much different from that of CMOS circuits [1].

In this paper we studied a VHDL behavioral model for NML circuits, which allows the evaluation of not only the logic behavior but also its power dissipation. It is based on technology solution called "Snake-clock."

Index Terms- Microprocessor, Nanomagnetic logic (NML), Null conventional logic (NCL), Power dissipation, Quantum-dot cellular automata (QCA), Very high speed integrated circuits hardware description language (VHDL).

I. INTRODUCTION

Quantum-dot cellular automata is a recent technology in which logic states are not stored as a voltage levels but as the position of individual electrons. QCA gives binary information by utilizing a bistable charge configuration instead of a current switch [2]. Currently it has two modes of implementations molecular QCA [8], [9] and magnetic QCA [10], based on domain nanomagnets, with only two stable magnetization states.

Another aspect of NML is that in order to propagate a signal without errors [16], an external field is applied which drives the cell in an intermediate unstable state lowering the potential barrier between the two stable magnetization values. When the field is removed magnets arrange themselves in ferromagnetic or antiferromagnetic manner depending upon the magnets relative placement. This magnetic field is called "*clock*". The necessity of clock signal and generated clock zones create a problem of "layout-timing." This problem can be unbearable in case of circuits with large number of gates and connections; hence there is solution termed as delay insensitive null convention logic (NCL) [22].

The various terms related to the paper are described in section II. Various circuits with advancements are mentioned in section III. The results of this literature survey are collected in section IV. The section V deals with the conclusion of this NML technology.

II. TERMINOLOGY

A. QCA

In quantum dot cellular automata, a QCA cell consists four *dots* that are positioned at corners of a square.

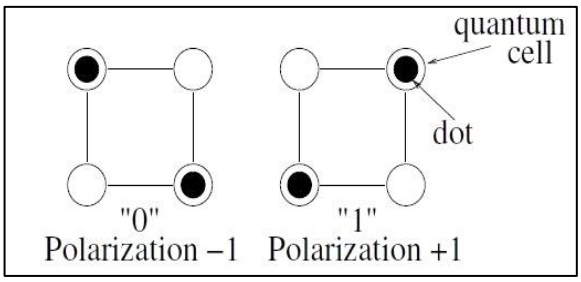

Figure 1: QCA cell [2]

A quantum dot is a site in a cell which a charge can be situated. The cell consists of two extra mobile electrons that can quantum mechanically tunnel between dots; but not cells. As shown in [Fig. 1] the two possible charge configurations are used to represent binary '0' & '1'[2].

In the molecular QCA the molecule has a bistable charge configuration in which binary information can be encoded. One molecule can be switched by a neighboring molecule [8], satisfying the key requirement for QCA operation. The simulation of molecular QCA wire is done in [9]. The magnetic QCA has received considerable attention because molecular QCA are currently far from technology reality; however the magnetic QCA or nanomagnetic logic (NML) allows fabrication of fully magnetic circuits with very low power consumption [2].

B. NML

Ferromagnetic and antiferromagnetic ordering in coupled nanostructures has recently received a considerable attention. These magnetic systems are adiabatically clocked by external magnetic field that enables the structures to relax their ground state from an initial metastable state. Certain arrangements of antiferromagnetically coupled dots are able to perform logical functionality called MQCA operation or NML. Recent experiments have shown correlation of 4-7 dots in a chain of single domain nanomagnets [10].

The basic cell is a single domain nanomagnet with aspect ratio which leads to shape anisotropy. This characteristic lets nanomagnets to have only two stable magnetizations, which represent the two logic values '0' & '1' [Fig. 2(a)]. The magnetization vector is parallel to the long side called as *easy axis* [13]. The magnetic field applied along short side which is called as *hard axis*.

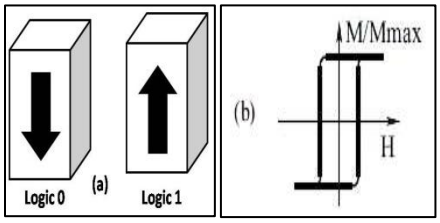

Figure 2: NML. (a) Single domain nanomagnets (b) Hysteresis loop of nanomagnets [13].

These two cells are separated by a potential barrier. When the field is applied the nanomagnets are forced into an unstable state, with the magnetization directed along the hard axis. The magnetic field is generated by a current flowing through a wire plates under magnets plane, and ferrite yoke is used [5]. As soon as the magnetic field is removed the magnets recognize themselves in an antiferromagnetic or ferromagnetic order [Fig. 3]. The alternating behavior of this field is the reason why it is called as "*clock*" [1]. Therefore, a complex circuit is divided into small structures called clock zones, which has small number of cells [13].

B. SNAKE CLOCK

As the external field is called clock, as it is iteratively switched on and off and allows the evaluation phase, even though it has not the "traditional" function of a clock signal. Hence the investigators have developed a solution to clock distribution, "snake-clock", which is more feasible for the multiple-phases clock [15] distribution, allows information propagation without losses in nanomagnets arrays [3].

The three phase snake-clock has *RESET, SWITCH, And HOLD* which is shown in [Fig. 4 (a)] both time and space. In [Fig. 4 (b)] the behavior of nanomagnets grouped in the corresponding clock zones is shown. In [Fig. 4 (c)] the top view of clock zones is shown. By this only *snake* like propagation is possible. Same can be observed by [Fig. 4 (d), (e)] [3].

C. NULL CONVENTIONAL LOGIC (NCL)

The use of a multiphase clock leads to the layout

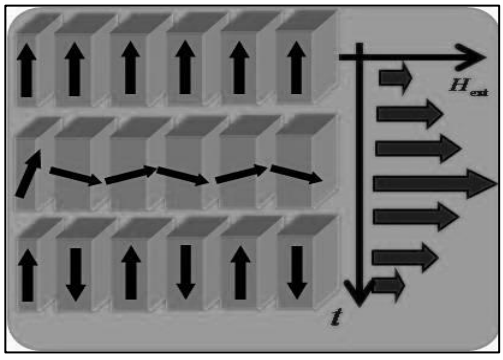

Figure 3: Magnets are forced in the unstable state when the magnetic field is applied [1].

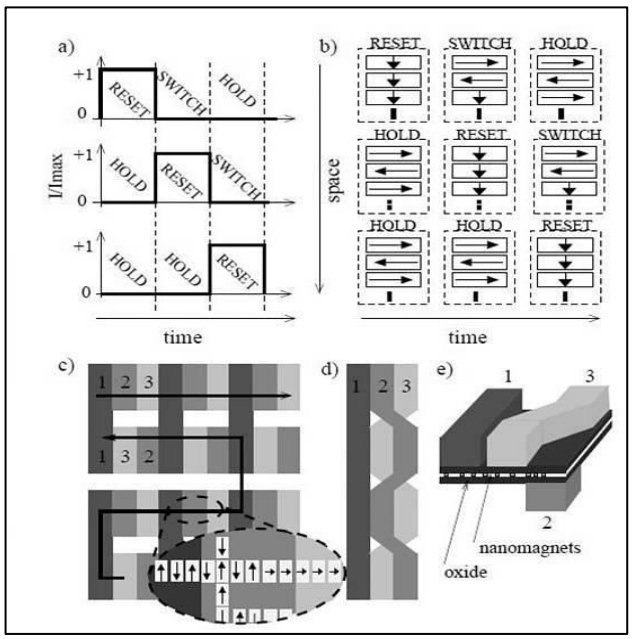

Figure 4: Snake Clock Organization [3], [4].

timing problem. As stated in [3] every clock zone is equivalent to a D-latch, where at every clock cycle the output copies the input value. Therefore, the propagation delay of a NML wire depends upon the number of clock zones the wire passes through. If different inputs signals of a gate arrive after an unequal number of clock cycles, the circuit will not work.

There is a solution called NCL [22]; which is an asynchronous delay-insensitive logic. Signals are coded using two bits, and they can assume two different states: NULL state when they are at same time 0; and DATA state which represents the logic value (01 means logic 0 and 10 means logic 1). The circuit passes from NULL to DATA only when all the inputs change from NULL to DATA and maintains its status until at least one input is in the DATA state. Before a new data can be accepted from a logic gate; every input must reach to the NULL state. Only at this point a new cycle can start. This ensures the circuit operations also in presence of a considerable difference in the propagation delay among the inputs [21].

III. CIRCUITS AND ADVANCEMENTS

A. BASIC STRUCTURES

Many works in the literature analyze the behavior of the basic blocks of this NML technology. The basic QCA cell can be combined to form a structure like a wire called "*QCA wire*" [2]. Similarly various types of QCA devices can be constructed using different physical cell arrangements. One of the basic logic gates in QCA is the "*Majority Voter"* with logic function *MV* (A, B, C) = AB + AC + BC. Majority voter can be realized by 5 QCA cells as shown in [Fig. 5] [13].

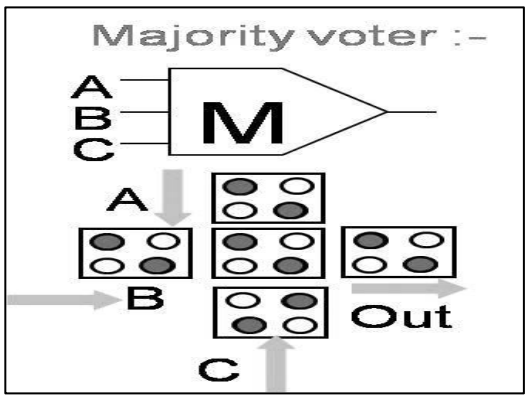

Figure 5: Majority voter: symbol and structure [2].

B. ADVANCEMENTS

From this basic gate various implementations are done like *QCA shift resister* [7]. The QCA latch is made up of three aluminum islands connected by tunnel junctions as shown in [Fig. 6]. A clock signal is applied to the middle dot to vary the potential on it so that it acts as a barrier for tunneling between the dots. Inputs are applied to the top and the bottom dots of latch by external input voltages. When no clock is applied and all the dots are neutral; the latch is in NULL state and holds no data.

As the clock signal is applied, the barrier height is increases, and the polarization of the latch takes on a definite value determined by the input. This is called as *"Active"* state. When the barrier height is large enough to suppress switching over the relevant time scale, hence the latch is in *"locked"* state. A shift register consists of a line of latches where each latch, in its locked state, acts as an input to the next. Binary information is transferred sequentially along the line from one latch to the next by applying a sequence of phase-shifted clock signals to successive latches. The clocking sequence and the resulting potentials in the shift register [7] are shown in [Fig. 7].

As moving further advancement in QCA designing; *QCA Adder* and *QCA Multiplier* are designed [14] by the investigators. They states that when circuits implemented using QCAs then there is significant complexity in interconnections and wire delay occurs.

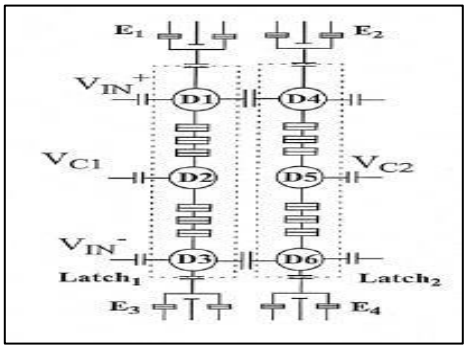

Figure 6: Schematic diagram of QCA shift resister [7].

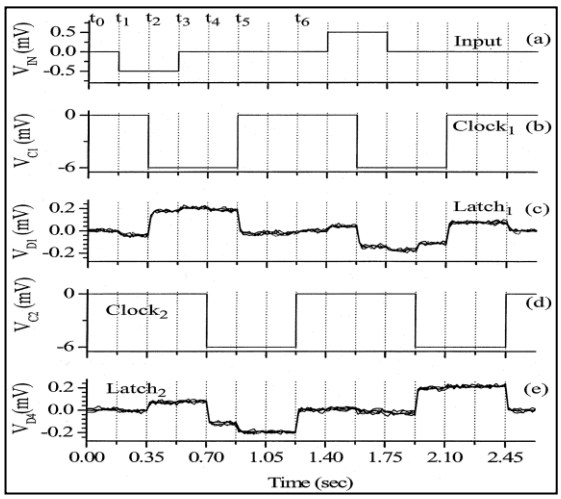

Figure 7: Operation of QCA shift register. (a) Input V_{1N} is applied to L_1. (b) Clock V_{C1} to latch L_1. (c) Output of L_1 measured by the potential on dot D_1. (d) phase-shifted clock V_{C2} applied to latch L_2. (e) Output of L_2 measured by the potential on dot D_4 [7].

In QCA, if the complexity increases, the delay may increase because of the increased cell counts and wired connections. They implemented new designs of Adder, the carry flow adder; [14] and serial parallel Multiplier network based on filter networks.

To prove the advancement in the QCA technology the comparison table between carry-look-ahead (CLA) adders and carry flow (CFA) adders is given in [Table I].

For the circuit layout and functionality checking, a simulation tool for QCA circuits was required. Hence a tool which is a product of an ongoing effort to create a rapid and accurate simulation layout tool for quantum-dot cellular automata (QCA) is developed known as QCADesigner [17]. QCADesigner is capable of simulating complex QCA designs on standard platforms. QCADesigner is a CAD tool designed specifically for QCA logic design and simulation. This tool allows the ability to layout and; verify a variety of QCA systems to users. This functionality occurs due to standard CAD features and various QCA specific simulation engines are provided in QCADesigner.

Table I: Adder comparisons [14]

	Complexity	Area	Delay
CLA4	1575 cells	$1.74\mu m \times 1.09\mu m$	$3\frac{2}{4}$ clocks
CLA8	3988 cells	$3.50\mu m \times 1.58\mu m$	$6\frac{2}{4}$ clocks
CLA16	10217 cells	$7.02\mu m \times 2.21\mu m$	$10\frac{1}{4}$ clocks
CLA32	25308 cells	$14.06\mu m \times 3.05\mu m$	19 clocks
CLA64	59030 cells	$28.20\mu m \times 3.73\mu m$	$31\frac{2}{4}$ clocks
CFA4	371 cells	$0.90\mu m \times 0.45\mu m$	$1\frac{2}{4}$ clocks
CFA8	789 cells	$1.79\mu m \times 0.53\mu m$	$2\frac{2}{4}$ clocks
CFA16	1769 cells	$3.55\mu m \times 0.69\mu m$	$4\frac{2}{4}$ clocks
CFA32	4305 cells	$7.09\mu m \times 1.03\mu m$	$8\frac{2}{4}$ clocks
CFA64	11681 cells	$14.15\mu m \times 1.71\mu m$	$16\frac{2}{4}$ clocks

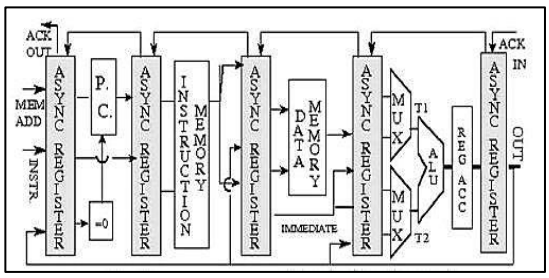

Figure 8: Architecture of microprocessor a NML [1].

Further improvements in QCA architectures are done gradually from a basic QCA cell to a NML microprocessor. The complete 4-bit microprocessor is a realistic architecture which was implemented in [1]. The processor architecture is simple but it can handle many types of operations: arithmetic, logic, memory read and write, and different kinds of jump. The microprocessor was chosen because it involves all types of logic circuits like combinational, sequential, etc. It represents the ideal testbench for the NML technology evaluation. The overall architecture of microprocessor is shown in [Fig. 8] [1]. There are four main blocks: a program counter (PC) which generates the address for the parallel instructions memory (16 words of 14 bits) and which manages jump instructions: a serial memory (4 words of 4 bits) for data storing; and finally a data- path block for the arithmetic operations. Two multiplexers select the ALU source operands, and an accumulator register stores ALU results. A comparator block maintains the conditional jumps. The comparator output is connected back to the jump enable of program counter.

C. POWER DISSIPATION

The energy dissipated during the magnetization reversal of larger size magnets is well known to be equal the area of the hysteresis loss as stated above. This "h*ysteresis loss*" originates from the irreversible change of complex domain pattern. Macro scale magnets dissipate power when their domain structures quickly rearrange in the presence of a varying external magnetic field. The energy dissipated from the microscopic model is the same as the area of hysteresis curve [12]. The energy of nanomagnet is shown in [Fig. 9].

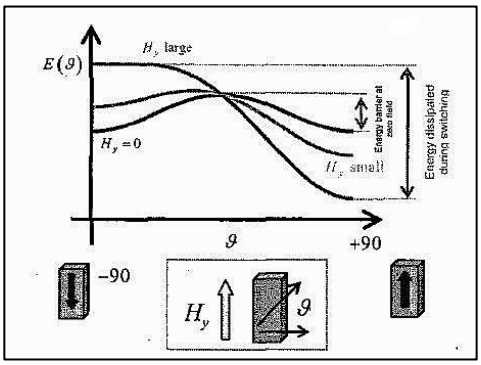

Figure 9: The energy of a nanomagnet [12].

Power losses in the NML circuits depend on two main components; power dissipated by nanomagnets during their switching phase, and power dissipated by clock wires during the reset field generation. During the switching the nanomagnet follows a hysteresis cycle as shown in [Fig. 2(b)]. The area of this hysteresis cycle is proportional to the energy spent for switching. This energy must be supplied to the nanomagnet by the source that generates the magnetic field, and this is normally dissipated in the form of heat.

The second one is the power dissipated by clock wires. This can be separated in two components: 1) the power dissipated because of the Joule effect and 2) the power stored in the wire inductance. The power dissipated by Joule effect represents the main contribution, mainly because a high value of current is necessary to generate a magnetic field strong enough to force a reset. The energy dissipated by the clock depends on the length of the wire, which is a function of the circuit area, affected by the circuit complexity and layout.

For the NML microprocessor a power model is made in [1] as shown in [Fig. 9]. The model is based on five key points as stated below;

1) It is embedded in the architecture description: Each block includes not only the logic sub-blocks but also the functions for evaluating the two power contributions.

2) It is hierarchical: A block of level N uses data on the number of magnets from sub-blocks of level $N-1$, and generates information to be propagated to the higher $N+1$ hierarchical level.

3) Given a block i in the architecture, a power estimator evaluates power consumption for current block i as a function of the number of nanomagnets in block i.

4) In the architecture of level N, a nanomagnet sum is enabled using the number of nanomagnets of all the included blocks of level $N-1$ as input. This sum is extended to each clock zone.

5) An overhead factor is used to take into account the routing complexity. If the sub-blocks have a total sum of magnets equal to M, the connection among them could require an additional number of magnets. This overhead is estimated and is multiplied by M. The value of this factor is different for each hierarchy level.

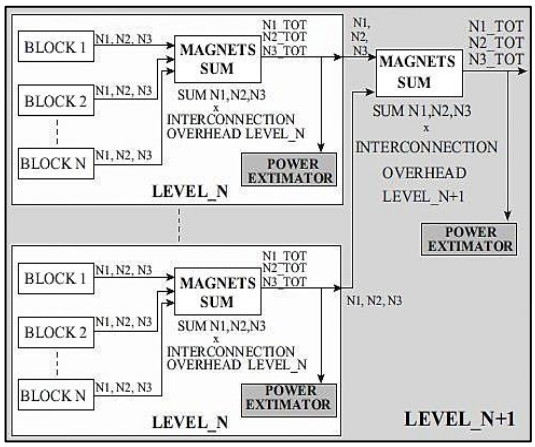

Figure 10: Hierarchical power model for microprocessor [1].

IV. RESULTS

As per the literature survey; many investigators provided a perspective of current-state nanoelectronic devices, which may a solution to the increasingly challenging manufacturing domain of conventional CMOS.

The [Fig. 11] shows the results of Majority voter; each map represents a combination of widths and lengths that corresponds to proper operation [13]. [Fig. 11(a)] shows the impact of sizes variation only of the Majority voter LEFT input magnet. It also shows that the aspect ratio should better remain near 2 or higher for a good rejection to process variations. [Fig. 11(b)] shows the influence of the sizes variations of DOWN input magnet on the whole gate behavior. The influence of UP input magnet is not recorded because it has the same behavior for symmetry. [Fig. 11(c)] shows the effect of the sizes variations of CENTRAL input magnet, which is responsible for the logic computation. [Fig. 11(d)] shows the influence of the same process variation applied to all magnets together.

To evaluate how the changes in the horizontal and vertical distances values affect performance, the 50% delay of the gate was measured. In case of NML technology, it is the delay between the 50% of the variation of the clock signal and the 50% of the variation of the magnetization of the CENTRAL block as shown in [Fig. 12] [13].

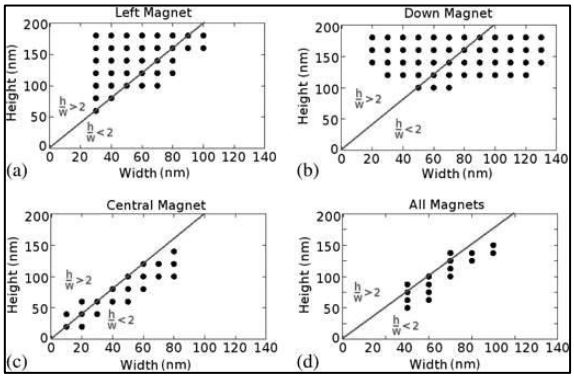

Figure 11: Majority voter working area considering process variations [13].

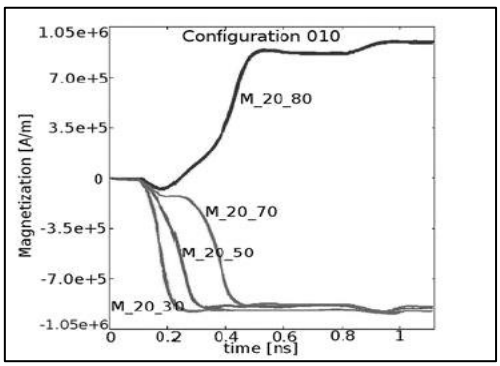

Figure 12: Timing variation of central magnet [13].

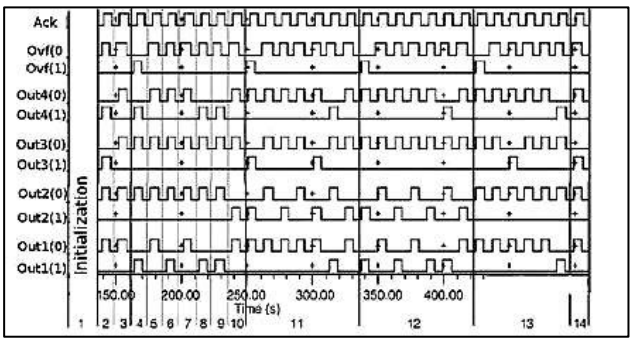

Figure 13: NML microprocessor modelsim simulation [1].

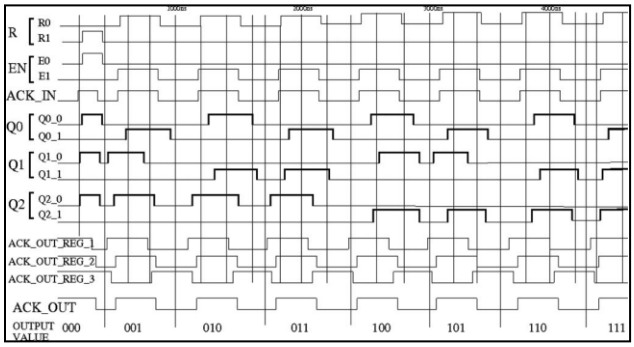

Figure 14: NCL counter simulation results [4].

Moving further with the complex circuit implementations; the QCADesigner came into focus. The QCADesigner needed because; the main problem in implementing more accurate simulations is the lack of experimental data for QCA systems with larger number of cells. The simulation results of NML microprocessor [1] are shown in [Fig. 13] using QCADesigner.

The null convention logic (NCL) counter is based on the generic structure of an NCL finite-state machine. A memory resister is used to store the present state, and a combinational circuit generates a future state [4]. NCL register don't have a memory function. Their aim is to implement the asynchronous communication protocol to guarantee delay insensitivity. The NCL counter simulation results are sown in [Fig. 14]. In this all the outputs switch from DATA state to NULL state and vice versa. The bold lines in the [Fig. 14] show when one of the bits assumes a DATA configuration. The entire structure works using *"snake-clock"*.

V. CONCLUSION

We studied various techniques developed by many investigators of nanomagnetic logic (NML) or magnetic quantum-dot cellular automata (QCA) circuits. These circuits are good for operation as they dissipate very low power as compared to traditional CMOS devices. We also come to know the terms like null conventional logic (NCL) and multiple phase clock i.e. snake clock.

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AUTHORS

First Author – Mr. M. B. Kachare, ME-Ist (Dig. Electronics), SSBT's COET, Bambhori, Jalgaon-425001, Maharashtra,India. mayur.kachare@rediffmail.com.

Second Author – Dr. P.H. Zope, Asst. Prof., SSBT's COET, Bambhori, Jalgaon-425001, Maharashtra,India. phzope@gmail.com

Correspondence Author – Mr. M. B. Kachare, ME-Ist (Dig. Electronics), SSBT's COET, Bambhori, Jalgaon-425001, Maharashtra,India. mayur.kachare@rediffmail.com., +919420499421.