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32-BIT MAC UNIT DESIGN USING VEDIC MULTIPLIER

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Abstract- This paper presents Multiply and Accumulate (MAC) unit design using Vedic Multiplier, which is based on Urdhva Tiryagbhyam Sutra. The paper emphasizes an efficient 32-bit MAC architecture along with 8-bit and 16-bit versions and results are presented in comparison with conventional architectures. The efficiency in terms of area and speed of proposed MAC unit architecture is observed through reduced area, low critical delay and low hardware complexity. The proposed MAC unit reduces the area by reducing the number of multiplication and addition in the multiplier unit. Increase in the speed of operation is achieved by the hierarchical nature of the Vedic multiplier unit. The proposed MAC unit is implemented on a field programmable gate array (FPGA) device, 3S100ETQ144-5 (Spartan 3). The performance evolution results in terms of speed and device utilization are compared to earlier MAC architecture. Though the use of Vedic mathematics methods for multiplication is reported in literature, it has been observed that our proposed method of 32-bit MAC unit implementation is using (32X32) multiplication unit and shows improvements in the delay and area.

Index Terms- MAC, Multiplier, Nikhilam Sutra, Urdhva Tiryagbhyam Sutra, Vedic Mathematics.

I. INTRODUCTION

The general MAC architecture consists of a conventional multiplier, adder and an accumulator. Where the output is added to the previous MAC output result by an accumulate adder. The Multiply-Accumulate (MAC) unit is extensively used in microprocessors and digital signal processors for data-intensive applications, such as filtering, convolution, and inner products. Most digital signal processing methods use nonlinear functions such as discrete cosine transform (DCT) or discrete wavelet transform (DWT) or FFT/IFFT computations that can be efficiently accelerated by dedicated MAC units. Because they are basically accomplished by repetitive application of multiplication and addition, the speed of the multiplication and addition determines the execution speed and performance of the entire computation. As the multiplier exhibits inherently long delay among the basic operational blocks in digital system, the multiplier determines the critical path.

In order to improve the speed of the MAC unit, there are two major bottlenecks. The first is the partial products reduction network that is used in the multiplication block and the second is the accumulator. Both of these stages require addition of large operands that involve long paths for carry propagation. The main key to the proposed architecture is using the Vedic multiplier to design the MAC unit and compare the performance with the conventional MAC units in terms of area, speed and number of resources.

High Speed Energy Efficient ALU design using Vedic multiplication techniques by the authors Ramalatha, M.Dayalan, K D Dharani, P Priya, and S Deoborah [2], wherein scope persists in further improving efficiency. It is well known fact that the speed of MAC is governed by the speed of the multiplier. The Vedic multiplier uses “Urdhva Tiryagbhyam” algorithm. The authors in [3] use Vedic multiplier based on the ancient algorithms (sutras) for multiplication. This work is based on the sutra "Nikhilam Sutra". This paper presents a technique to modify the architecture of the Vedic multiplier by using existing methods in order to reduce power. The proposed design shows considerable improvements in terms of power.

The remainder of this paper is organized as follows, Section 2 describes Overview of Vedic Mathematics. Section 3 Review of Multipliers. Section 4 describes the MAC architecture unit. Section 5 describes the Results and Discussion. Section 6 presents the Conclusion drawn in this work.

II. VEDIC MATHEMATICS

The Sanskrit word ‘Veda’ means ‘knowledge’. The Vedas consist of a huge number of scriptures. There are thousands of documents in Indian scriptures, and much part of it is yet to be translated. These scriptures are highly structured, both within themselves and in relation to each other. Some documents, called **‘**Ganita sutras’ (the name ‘Ganita’ means mathematics), were devoted to mathematical knowledge. Sri Bharati Krishna Tirtha Maharaj, who is considered the doyen of this discipline, in his seminal book Vedic Mathematics, wrote about this special use of sutras. Vedic Mathematics" was the name given by him. He cognized the lost formulae from the scriptures of "Atharva Vedas" and compiled them in the form of Sixteen Sutras and thirteen sub-sutras. Vedic Mathematics is based on 16 sutras dealing with mathematics related to arithmetic, algebra, and geometry, which can further be extended to any area of Applied and Pure Mathematics.

III. MULTIPLICATION

Multiplication is a fundamental operation of MAC unit [1]. Multipliers have large area, long latency and consume considerable power. Fast multipliers are essential parts of digital signal processing systems. In order to improve the speed of the MAC unit, there are two major criteria's. The first is reducing the number of partial products in the multiplication block and the second is reducing burden of accumulator. As the multiplier consumes considerable delay among the basic operational blocks in digital system, the multiplier determines the critical path. In this section the MAC using the Vedic, Booth and Conventional multiplier is discussed.

3.1 Vedic Multiplier

The main purpose of Vedic Mathematics is to be able to solve complex calculations by simple techniques. The formula being very short makes them practically simple in implementation. Urdhva-tiryagbhyam (Vertically and crosswise) sutra is general formula applicable to multiplication operation. Its algebraic principle is based on multiplication of polynomials. The Vedic multiplier using Urdhva-tiryagbhyam sutra of width NXN will generate the 2N-1 cross products of different widths which when combined forms ($\log_2 N + 1$) partial products. The partial products are obtained by vertical and crosswise operations using the Sutra. Hence the delay is equal to adder delay. Critical path would consist of adders adding the maximum number of bits in cross product. In all cases it will be the cross product in which all bits of multipliers are considered.

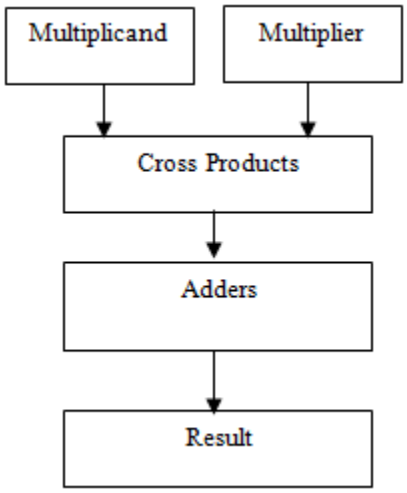

Fig 1. Architecture of Vedic Multiplier.

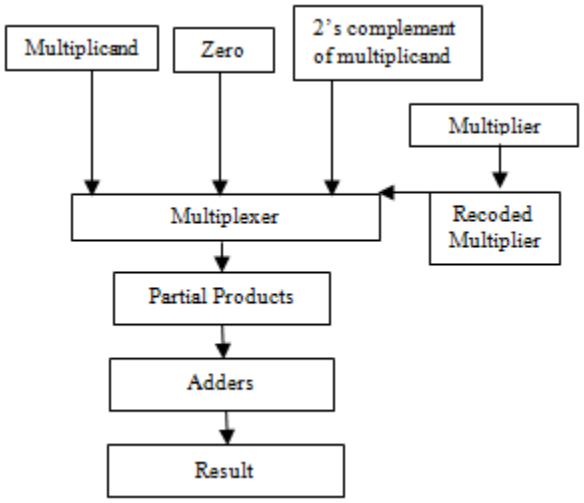

Fig 2. Architecture of Booth Multiplier

3.2 Booth Multiplier

The Booth multiplier is also known as Recoded booth multiplier, in which the multiplicand is kept as it is and the multiplier is recoded as a recoded multiplier and then the multiplication is done with multiplicand and recoded multiplier. To reduce the number of partial products in the multiplier, the Multiplier uses Radix 2^r multipliers, which produces *N/r* partial products, each of which depends on *r* bits of the multiplier. Fewer partial products lead to a smaller and faster CSA (Carry Save Adder) array. For example, a radix-4 multiplier produces N/2 partial products. Each radix-4 multiplier produces N/2 partial products. Each partial product is 0, Y, 2Y, or 3Y,depending on a pair of bits of X. Computing 2Y is a simple shift, but 3Y is a hard multiple requiring a slow carry-propagate addition of Y + 2Y before partial product generation begins. Higher-radix Booth encoding is possible, but generating the other hard multiples appears not to be worthwhile for multipliers of fewer than 32 bits. The figure 2 shows the basic architecture of Booth multiplier.

3.3 Conventional Multiplier

The conventional multiplier of width N x N bits will generate the N number of partial products. The partial products are generated by bit wise ANDing one multiplier bit with another multiplier. Hence, the N x N bit multiplier uses 2N-multiplications and N-Adders in the architecture of Conventional multiplier. Fig. 4 below shows the basic architecture of conventional multiplier. The Multiplications and Additions are significantly reduced in case of Vedic Multiplier compared to Booth and conventional multiplier. Table 1 gives details about the Hardware resources used i.e., Multiplications and Additions in case of Vedic, Booth and conventional multiplier for 8x8-bit, 16x16-bit & 32x32-bit.

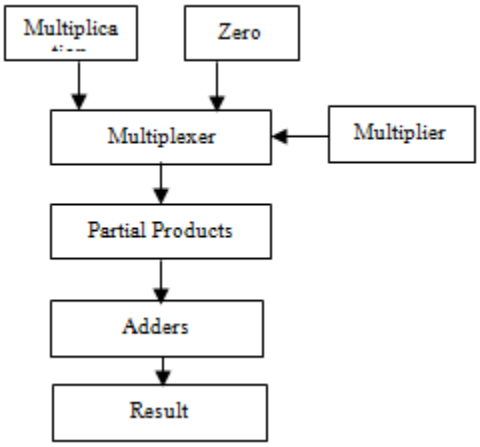

Fig.3 Architecture of conventional multiplier.

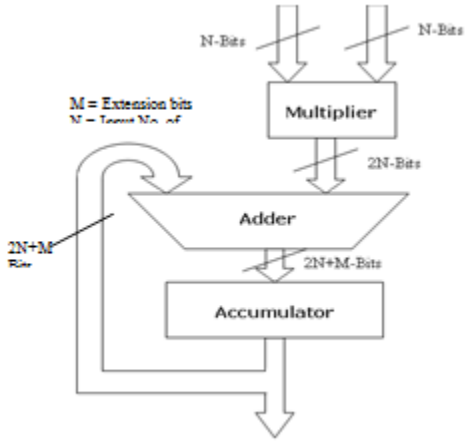

Fig.4 Architecture of MAC Unit

Table 1: Number of Additions and Multiplications in multipliers

Multiplier Unit	8x8-bit	16x16-bit	32x32-bit
Conventional	64-M 56-A	256-M 240-A	1024-M 1022-A
Booth	40-M 26-A	96-M 72-A	288-M 243-A
Vedic	8-M 4-A	16-M 8-A	32-M 16-A

In the Table 1, 'M' stands for multiplications used in the respective width of multipliers and 'A' stands for additions used in the respective width of multipliers.From this Table 1 it is clear that how the Vedic mathematics going to reduce the number of adder and multiplier as compare to the conventional and Booth multiplier. As we are reducing the number of adder in each bit the delay provided by the particular circuit is also going to reduced hence, which causes to increases the speed of MAC unit

The objective of a good multiplier is to provide a physically compact, improved and occupying less area. In this paper, we propose a high-speed area efficient Multiply and Accumulate unit (MAC) adopting Vedic multiplication sutra based architecture for 8 bit, 16 bit and 32 bit size.

IV. MULTIPLY ACCUMULATE UNIT

Multiplication Accumulation is an important part of real-time digital signal processing (DSP) with applications ranging from digital filtering to image processing. Multiply and accumulate is a very common basic-level operation seen in many DSP designs/algorithms. Two numbers are multiplied together, and added into an accumulator register. As shown in Fig.4, the basic MAC unit consists of multiplier, adder and accumulator. In general MAC unit uses the conventional multiplier unit, which consists of multiplication of multiplier and multiplicand based on adding the generated partial products and to compute the final multiplication. This results to adding the partial products. The key to the proposed MAC unit is to enhance the performance of MAC using Vedic Multiplier and to compare the Vedic, Booth and conventional multiplier in terms of computation required to generate the partial products and add the generated partial products to get the final result of the multiplication.

V. RESULTS AND DISCUSSION

The algorithm is designed for 32-bit input using Verilog-HDL. Simulation is done using Xilinx ISE 12.3. Synthesis and Implementation is done using Xilinx, Device Family: Spartan 3, Device: XCS100e, Package: tq144, Speed grade: -5. The device is made up of multiplexers and LUTs.

Table 2: Comparison of combinational path delay

Bit width size	Delay of optimized Vedic multiplier in ns described in [2] [Device Spartan 2S200PQ208-6]	Delay of proposed MAC in ns [Device Spartan 3S100ETQ144-5]
16-bit	22.604	10.213

32-bit	35.76	14.69

The subsequent figures show the simulation results, the Fig. 5 gives the RTL schematics, the Fig.6 shows Technical Schematic and the Fig.7 gives the simulation waveform output of 32-bit MAC Unit using Vedic Multiplier.

Table 2 gives the comparison of combinational path delay of the proposed MAC module with optimized Vedic multiplier discussed in [2]. It is observed that for 16 and 32-bit proposed MAC module, the gate delay are 10.213ns,and 14.69ns while it is 22.604 ns, and 35.76 ns for the corresponding optimized Vedic multiplier described in [2].

The Fig.8 gives the speed comparison of N-bit MAC unit and also given the results for the 8-bit, 16-bit & 32-bit MAC Unit and from the Fig.8 it can be observed that as the number of bit increase the delay increases. The Fig.9 gives the area comparison of N-bit MAC unit and also shows the results for 8-bit, 16-bit & 32-bit MAC unit, it is observed that as the number of bits increases the area utilized also increases.

Table 3: Comparison of synthesis results

MAC Unit	8-bit	16-bit	32-bit
Delay	6.728 ns	10.213 ns	14.69 ns
Number of slices	44 out of 960 4%	94 out of 960 9%	203 out of 960 21%
Number of LUTs	69 out of 1920 3%	139 out of 1920 7%	313 out of 1920 16%

Table 3 shows the comparison of synthesis results of 8-bit, 16-bit and 32-bit, MAC architecture. For 8-bit MAC, the gate delay in the architecture is 6.728 ns with nearly 3% device utilization (number of slices: 44 out of 960 4% and number of 4_input LUTs: 69 out of 1920 3% . For 16-bit MAC, the gate delay in the architecture is 10.213 ns with nearly 7% device utilization (number of slices: 94 out of 960 9% and number of 4_input LUTs: 139 out of 1920 7% . For 32-bit MAC, the gate delay in the architecture is 14.69 ns with nearly 7% device utilization (number of slices: 203 out of 960 21% and number of 4_input LUTs: 313 out of 1920 16% .

Simulation and synthesis results show the comparison between conventional MAC and Vedic MAC in terms of delay and area. This is shown by bar-graph. The following bar-graph shows that there is some reduction in delay and area which means overall performance of Vedic MAC is better than the conventional MAC.

Since the speed and chip area are important considerations in Microprocessors and various DSP applications, the MAC will be optimized for maximum throughput in a fixed area. The pipeline technique is widely used to improve the performance of digital circuits. We use pipelined architecture to achieve our goal of maximum throughput and used to accelerate the multiplication speed. As the number of pipeline stages is increased, the path delays of each stage are decreased and the overall performance of the circuit is improved.

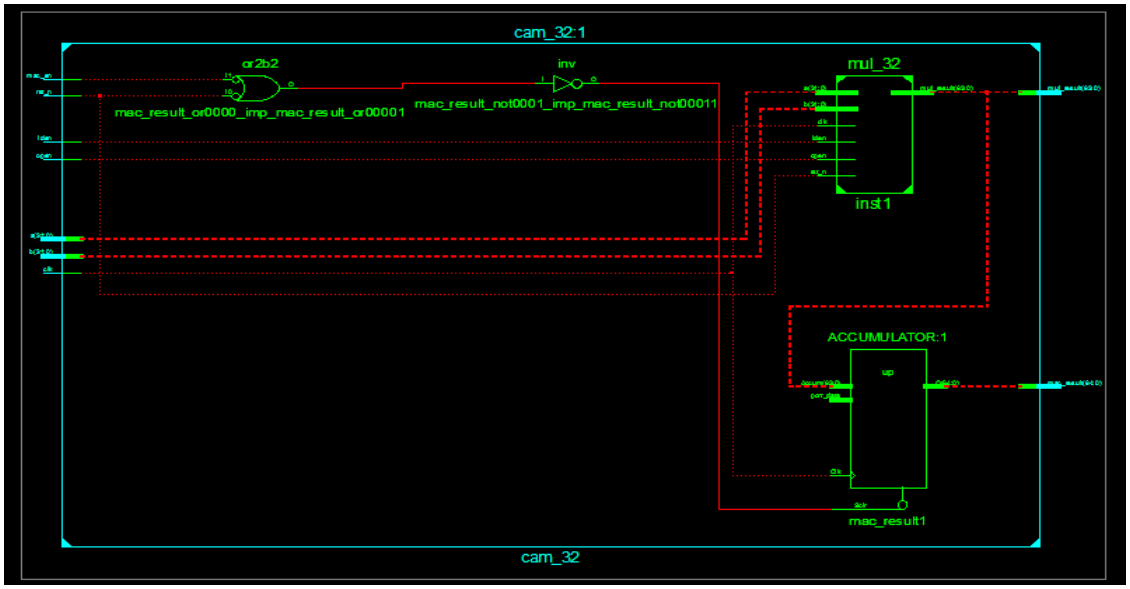

Fig 5. RTL schematic of proposed 32-bit Vedic multiplier

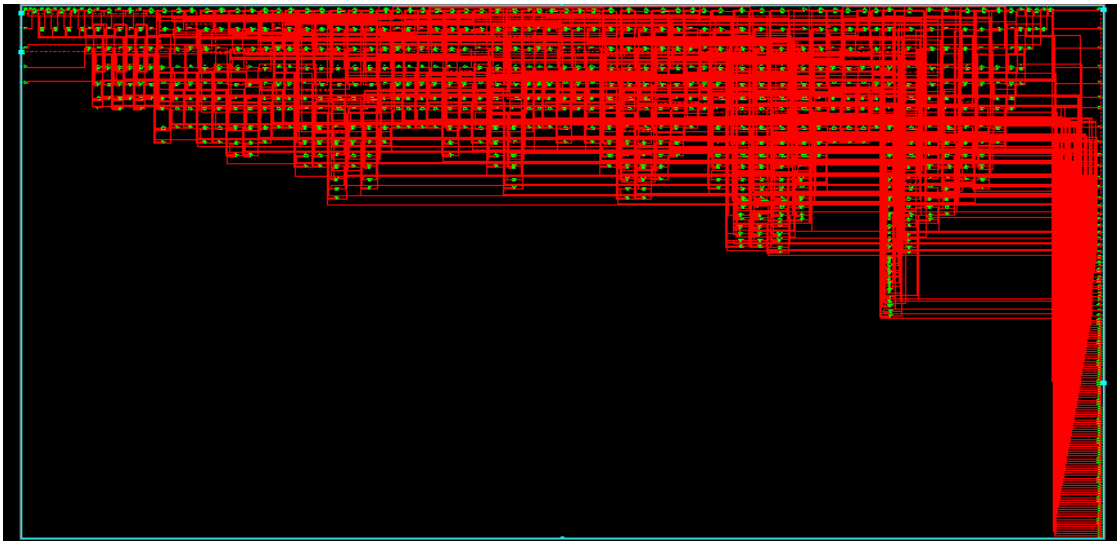

Fig 6. Technology Schematic of 32-bit MAC Unit

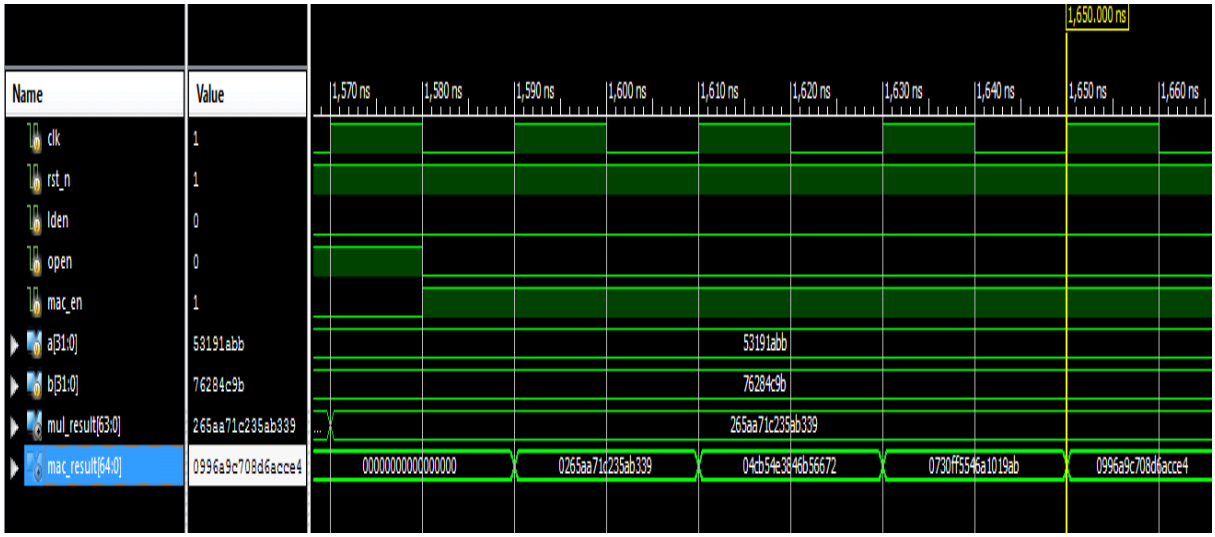

Fig 7. Simulation w/f of proposed 32-bit MAC Unit

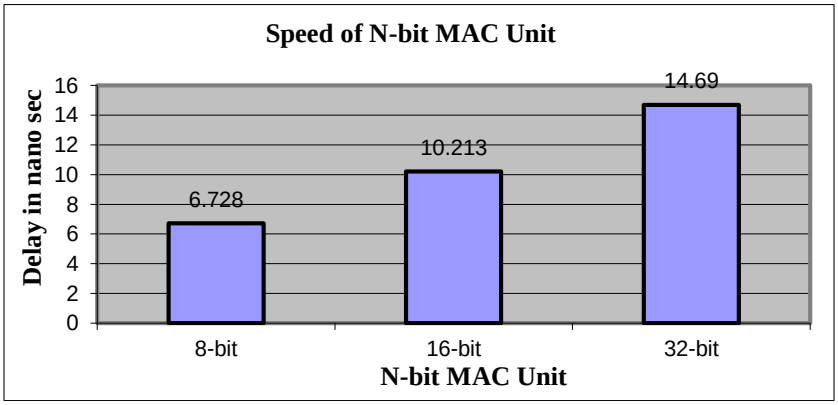

Fig 8. Speed of N-bit MAC Unit

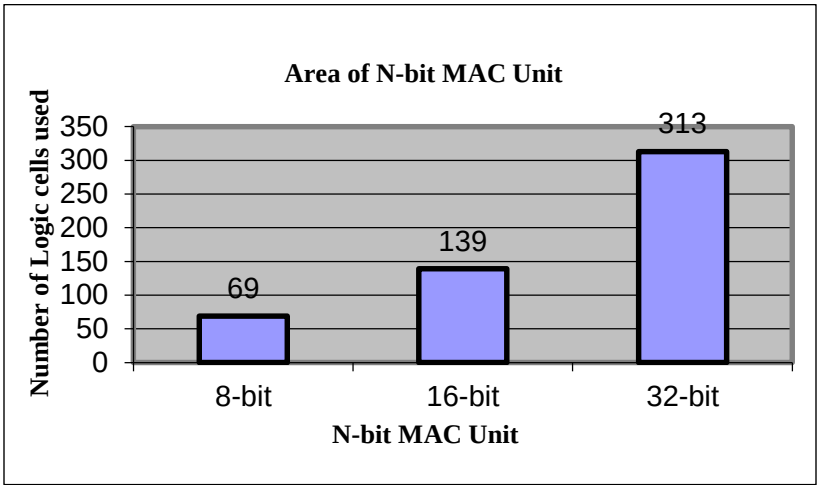

Fig 9. Area of N-bit MAC Unit

VI. CONCLUSION

The results obtained are quite encouraging. The 8-bit, 16-bit & 32-bit multiplier-accumulators (MAC) unit using Vedic multiplier is presented in this work. The basic building blocks for the MAC unit are identified and each of the blocks is analyzed for its performance. It can be concluded that 32-bit MAC using vedic Multiplier is superior in all respect like speed, delay, area, complexity compared to [2].

Research is going on towards the implementation of the reconfigurable 32-bit MAC architecture using 4-bit, 8-bit, 16-bit as basic building blocks. This also gives chances for modular design where smaller block can be used to design the bigger one. So the design complexity gets reduced for inputs of large no of bits and modularity gets increased. The application of transform algorithm includes linear filtering, Correlation, Spectrum Analysis which will further adds the field of Communication, signal & image processing and instrumentation that can also benefit future needs of wireless communications systems. Combine approach of transform algorithms with Vedic Mathematics create the new advancement in various fields of engineering.

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