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STUDY OF VLSI BULK CMOS AND SOI TECHNOLOGIES

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Abstract- The paper reviews the basic circuit issues of the bulk and SOI technology, and also shows the superior features of SOI which include the process and developing circuits. And finally, conclusion shows the comparison of two technologies by giving the appropriate design description.

Index Terms- Bulk CMOS technology, SOI technology.

I. INTRODUCTION

The process of designing digital hardware has changed dramatically over the past few years. Unlike previous generations of technology, in which board-level designs included large numbers of SSI chips containing basic gates, virtually every digital design produced today consists mostly of high-density devices. Where the high density devices are developed by VLSI, this introduces the incorporating of several numbers of transistors on a single chip. According to MOORES Law the count of transistors are doubled for every six months, which gives the high reliability and better performance. This applies not only to custom devices like processors and memory, but also for logic circuits such as state machine controllers, counters, registers, and decoders. When such circuits are destined for high-volume systems they have been integrated into high-density gate arrays. And the paper introduces the two technologies i.e. Bulk CMOS and SOI CMOS technology, considering these two to technologies the paper is further processed by giving the brief description of each technology and the needs, effects and application are discussed.

II. SEMICONDUCTORS

A semiconductor has two types of mobile charge carriers: negatively charged electrons and positively charged holes. We shall denote the concentrations of these charge carriers by n and p respectively. The discussions in this booklet apply to elemental semiconductors (like silicon) which belong to group IV of the periodic table. We can intentionally add impurities from groups III and V to the semiconductor. These impurities are called dopants. Impurities from group III are called acceptors while those from group V are called donors. Each donor atom has an extra electron, which is very loosely bound to it. At room temperature, there is thermal energy present, so that the loosely bound electron breaks free from the donor, leaving the donor positively charged. This contributes an additional electron to the free charge carriers in the semiconductor, and a positive ionic charge at a fixed location in the semiconductor. Similarly, an acceptor atom captures an electron, thus producing a mobile hole and becoming negatively charged itself. A semiconductor without any dopants is called intrinsic. An unperturbed semiconductor must be charge neutral as a whole. If we denote the concentration of ionised donors by N_d^+ and the concentration of ionised acceptors byN_a^-, we can write for the net charge density at any point in the semiconductor as.

$$\rho = q(N_d^+ - N_a^- + p - n) \quad (1)$$

Where q is the absolute value of the electronic charge. In an unperturbed semiconductor, will be zero everywhere. Electrons and holes are generated thermally – the availability of energy equal to the band gap of the semiconductor results in the generation of an electron - hole pair. Simultaneously, electrons and holes can recombine to annihilate each other, giving out energy which is equal to the band gap of the semiconductor. Thus we have the reversible reaction:

$$e^- + h^+ \leftrightarrow E_g \quad (2)$$

Where Eg is the band gap energy of the semiconductor. Applying the law of mass action to the above reaction, we can write for the equilibrium concentration of holes and electrons:

$$n.p = constant \quad (3)$$

The above relation applies to doped as well as intrinsic semiconductors. But for an intrinsic semiconductor,

$$n = p \equiv n_i \quad (4)$$

Therefore, the constant in the equation connecting n and p must be n. Thus, for a semiconductor in equilibrium,

$$n.p = n_i^2 \quad (5)$$

Since n and p are not independent, but are constrained by the above relation, we can define a single independent variable, the Fermi potential by (9, 10)

$$\emptyset_F \equiv \frac{K_B T}{q} ln \frac{p}{n_i} = \frac{K_B T}{q} ln \frac{n_i}{n_i} \quad (6)$$

Where KB is the Boltzmann constant, T is the absolute temperature and q is the absolute value of the electronic charge. At room temperature, K_BT=q is approximately 26 mV and n_i is

of the order of 10^{10}=cm3 for silicon. Now electron and hole concentrations are given by:

$$n = n_i e^{-q\emptyset_F}/K_B T \quad (7)$$

$$p = n_i e^{q\emptyset_F}/K_B T \quad (8)$$

$$n = n_i e^{-uF} \quad (9)$$

$$p = n_i e^{uF} \quad (10)$$

Table 1 Semiconductor band gap

Material	Energy gap (eV)	
	0K	300K
Si	1.17	1.11
Ge	0.74	0.66
InSb	0.23	0.17
InAs	0.43	0.36
InP	1.42	1.27
GaP	2.32	2.25
GaAs	1.52	1.43
GaSb	0.81	0.68
CdSe	1.84	1.74
CdTe	1.61	1.44
ZnO	3.44	3.2
ZnS	3.91	3.6

Table 2 Semiconductor Properties: Band Gaps, Effective Masses, Dielectric Constants

Semiconductor	Energy gap (eV) at 273 K	Effective mass m*/m		Dielectric constant
		Electrons	Holes	
Ge	0.67	0.2	0.3	16
Si	1.14	0.33	0.5	12
InSb	0.16	0.013	0.6	18
InAs	0.33	0.02	0.4	14.5
InP	1.29	0.07	0.4	14
GaSb	0.67	0.047	0.5	15
GaAs	1.39	0.072	0.5	13

The above table 1 shows the band gap of several semiconductor materials, but table 2 gives the semiconductor properties of semiconductor materials, which are continuously used in Integrated circuits fabrication process, depending upon on the application, respective material are preferable.

III. WHY SILICON [$S^{14}_{28.09}$]?

Quartz (crystalline silicon dioxide) has been known to people for many thousands of years. Flint is a form of quartz, and tools made from flint were in everyday use in the Stone Age.

In 1789, the French chemist Antoine Lavoisier proposed that a new chemical element could be found in quartz. This new element, he said, must be very abundant. (1) He was right, of course. Silicon accounts for 28% of the weight of Earth's crust.

Silicon was given its name in 1831 by Scottish chemist Thomas Thomson. He retained part of Berzelius's name, from 'silicis,' meaning flint. He changed the element's ending to on because the element was more similar to nonmetals boron and carbon than it was to metals such as calcium and magnesium. (Silicis, or flint, was probably our first use of silicon dioxide. (11-14))

- The lowest acceptable purity for electronic grade silicon is 99.9999999%. This means that for every billion atoms, only one non-silicon atom is allowed.
- Silicon is the second most abundant element in our planet's crust. Oxygen (47.3%) and silicon (27.7%) together make up 75% of the weight of Earth's crust. Most of the crust's silicon exists as silicon dioxide; we are familiar with this as sand or quartz.

3.1 CHARACTERISTICS

- Silicon is a hard, relatively inert metalloid and in crystalline form is very brittle with a marked metallic luster.
- Silicon occurs mainly in nature as the oxide and as silicates.
- The solid form of silicon does not react with oxygen, water and most acids.
- Silicon reacts with halogens or dilute alkalis.
- Silicon also has the unusual property that (like water) it expands as it freezes.
- Four other elements expand when they freeze; gallium, bismuth, antimony and germanium

3.2 USES OF SILICON

- Silicon chips are the basis of modern electronic and computing. The silicon must be ultrapure, although depending on final use it may be doped with part per million levels of arsenic, boron, gallium, germanium, or phosphorus.
- Silicon is alloyed with aluminium for use in engines as the presence of silicon improves the metal's castability. Silicon can enhance iron's magnetic properties; it is also an important component of steel, which it toughens.
- Silicon carbide, more commonly called carborundum, is extremely hard and is used in abrasives.
- Silica (SiO_2) in sand and minerals in clay is used to make concrete and bricks. Silica, as sand, is also the main constituent of glass.
- Pure, crystalline silicon dioxide (quartz) resonates at a very precise frequency and is used in high-precision watches and clocks.

- Silicones are important silicon based polymers. Having heat-resistant, non-stick, and rubber-like properties, silicones are often used in cookware, medicine (implants), and as sealants, adhesives, lubricants, and for insulation
- Pure silicon is easily available cost is less efficient fabrication techniques for silicon processing better mechanical and physical properties of silicon integration with control and signal processing circuitry.

IV. CMOS TECHNOLOGY

For semiconductor integrated circuits, during the past decades, the CMOS technology emerged as the dominant fabrication method, and CMOS became the almost exclusive choice for semiconductor memory designs also. With the development of the CMOS memory technology numerous publications presented select CMOS memory circuit- and architecture-designs, but these disclosures, sometimes for protection of intellectual property, left significant hollows in the acquainted material and made little attempt to provide an unbiased global picture and analysis in an organized form. Furthermore, the analysis, design and improvement of many memory-specific CMOS circuits, e.g. memory cells, array wiring, sense amplifiers, redundant elements, etc., required expertness not only in circuit technology, but also in semiconductor processing and device technologies, modern physics and information theory. The prerequisite for combining these diverse technological and theoretical sciences from disparate sources made the design and the tuition of CMOS memory circuits exceptionally demanding tasks. Additionally, the literature of CMOS technology made little effort to give overview texts and methodical analyses of some significant memory-specific issues such as sense amplifiers, redundancy implementations and radiation hardening by circuit-technical approaches.(6,8)

Since the combination of radiation hardness and high performance was the incipient stimulant to develop CMOS silicon-on-insulator SOI and silicon-on-sapphire SOS memories, this closing chapter devotes a substantial part to the peculiarities of the CMOS SOI (SOS) memory circuit designs. The circuits and architectures presented in this original monograph are specific to CMOS nonprogrammable write-read and read-only memories. Circuits and architectures of programmable memories, e.g. PROMS, EPROMs, EEPROMs, NVROMs and Flash-Memories are not among the subjects of this volume, because during the technical evolution programmable memories have become a separate and extensive category in semiconductor memories. Yet, a multitude of programmable and other semiconductor memory designs can adopt many of the circuits and architectures.

As CMOS technology is the basic semiconductor model CMOS IC are almost exclusively fabricated on bulk silicon substrate, for two well known reasons: the arability of electronic grade material produced either by the Czochralski of floating gate technique, and because good quality oxide can be readily grown on silicon, a thing is not possible on germanium or on compound semiconductor. ic grade material produced either by the Czochralski of floating gate technique, and because good quality oxide can be readily grown on silicon, a thing is not possible on germanium or on compound semiconductor. Modern MOSFET'S made in bulk silicon Far from the ideal structure described by Lilienfield. Bulk MOSFET'S are made in silicon wafers having a thickness of approximately 800 micrometer, but only the first micrometer at the top of the wafer is used for transistor fabrication. Interactions between the devices and the substrate give rise to a range of unwanted parasitic effects.(15,16)

One of these is a parasitic capacitance between diffused source and drain and the substrate. This capacitance increases the substrate doping, and become large in submicron devices where doping concentration in the substrate is higher in previous MOS technologies. Source and drain capacitance consists not only in obvious capacitance of the depletion regions associated with the junctions, but also in the capacitance between the junction and heavily doped channel stop located underneath the field oxide. Latchup, which consists of unwanted triggering of PNPN thyristor structure inherently present in all bulk CMOS structure, becomes a several problem in devices with small dimensions, where the gain of parasitic bipolar devices involved in the parasitic thyristor becomes larger.

The MOSFET works in three regions ie cut-off, linear and saturation region they have given names depending upon the flow of electronics and the applied threshold and gate voltage.

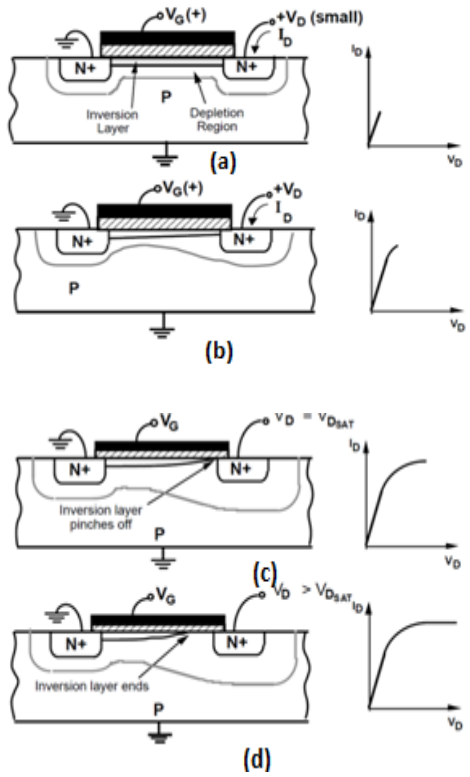

Fig 1 CMOS in 3 different regions and their VI characteristics (a) cut-off, (b) linear, (c) saturation, (d) saturation in pinch-off condition

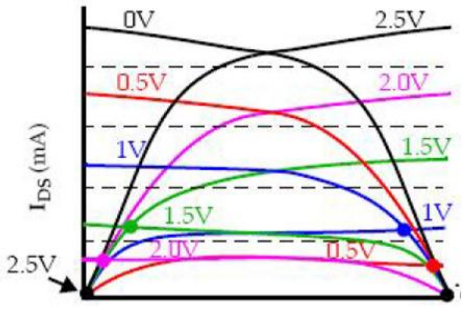

Fig2 Currents of PMOS and NMOS

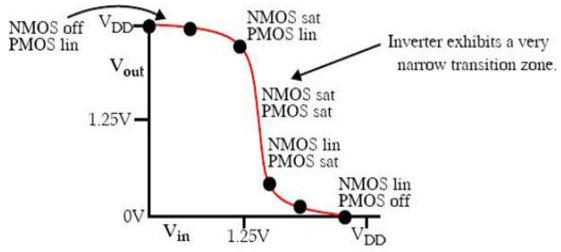

Fig 3 Dynamic characteristics of CMOS Inverter

Table 3 Relations between voltages for the three regions of operation of CMOS inverter

	Cut-off	Non-saturated	Saturated
P-device	$V_{gsp}>V_{tp}$ $V_{in}>V_{tp}+V_{dd}$	$V_{gsp}<V_{tp}$ $V_{in}<V_{tp}+V_{dd}$ $V_{dsp}>V_{gsp}-V_{tp}$ $V_{out}>V_{in}-V_{tp}$	$V_{gsp}<V_{tp}$ $V_{in}<V_{tp}+V_{dd}$ $V_{dsp}<V_{gsp}-V_{tp}$ $V_{out}<V_{in}-V_{tp}$
N-device	$V_{gsn}<V_{tn}$ $V_{in}<V_{tn}$	$V_{gsn}>V_{tn}$ $V_{in}>V_{tn}+V_{dd}$ $V_{dsn}<V_{gsn}-V_{tn}$ $V_{out}<V_{in}-V_{tn}$	$V_{gsn}>V_{tn}$ $V_{in}>V_{tn}+V_{dd}$ $V_{dsn}>V_{gsn}-V_{tn}$ $V_{out}>V_{in}-V_{tn}$

V. SOI TECHNOLOGY

The idea of realizing semiconductor devices in a thin silicon film is mechanically supported by an insulating substrate has been around for several decades. The first description of the insulated gate field effect transistor (IGFET), which evolved in to the modern silicon metal oxide semiconductor field effect transistor, is found in the historical patent of Lilienfield in 1926. This patent depicts a three terminal device where the source to drain current is controlled by field effect from a gate, dielectrically insulated from the rest of the devices. The piece of the semiconductor which constituted the active part of the device was a thin semiconductor film deposited on a insulator. In a sense, it can thus be said that a first MOSFET semiconductor on insulator device. The technology of that time was unfortunately was unable to produce a successfully operating Lilienfield device. IGFET technology was then forgotten for a while completely overshadowed by the enormous success of the bipolar transistor discovered in 1947.(1-5)

SOI CMOS technology is also attractive because it involves less processing steps the bulk CMOS technology and because it is suppressed some yield hazard factors present in bulk CMOS. To illustrate this we can take the example of realizing a shallow junction and making contact to it. Making shallow junction is not a obvious task in bulk CMOS. If a thin SOI substrate is used, on the other hand, the depth of the junction will automatically be equal to the thickness of silicon film. Electric contact to a shallow junction can be made using a metal, an alloy or a metal silicide. In bulk silicon devices, unwanted reactions can take place between the silicon and the metal or the silicide, such that the metal "punch through" the junction. This effect is well known in the case of aluminium, but can also occur with the metal or slicide systems. Such a junction punches through give rise to uncontrolled leakage currents. If the devices are realized in thin SOI material, the N^+ or P^+ source and drain diffusion extend to buried insulator. In this case there, is no metallurgical junction underneath the metal silicon contact area, and no leakage will be produce if some uncontrolled metal silicon occurs.

The absence of latch up, reduced parasitic source and drain capacitance, and easy of making of shallow junctions are the examples of advantages of SOI over bulk. There are many other properties which allows SOI device and circuits to exhibit performances superior to those of their bulk counter parts (radiation hardness, high temperature, improve trance conductance and subthreshold slop,….)

VI. SOI BASIC

In a Silicon On Insulator (SOI) Fabrication technology, transistors are built on a silicon layer resting on an Insulating Layer of Silicon dioxide (SiO2). The insulating layer is created by flowing oxygen onto a plain silicon wafer and then heating the wafer to oxidize the silicon, thereby creating a uniform buried layer of silicon dioxide. Transistors are encapsulated in SiO2 on all sides. The below figure shows a typical NMOS Transistor with Bulk CMOS Process and with SOI Process.

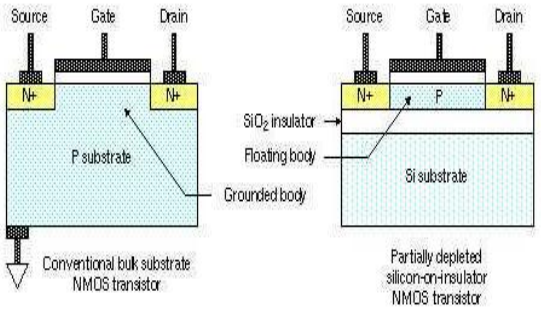

Figure 4 Bulk NMOS Transistor vs SOI NMOS Transistor.

The insulating layer increases device performance by reducing junction capacitance as the junction is isolated from bulk silicon. The decrease in junction capacitance also reduces overall power consumption.

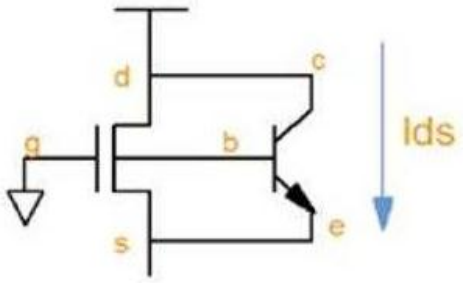

Figure 5 Bipolar current of the SOI FET

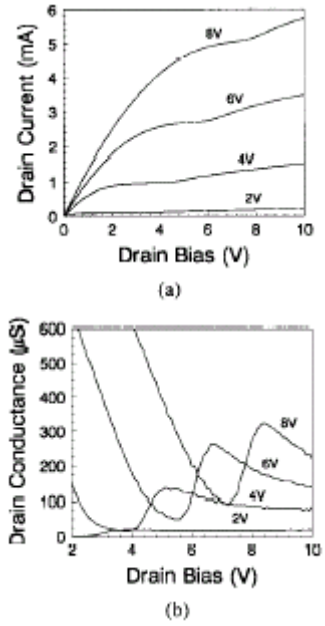

Figure 6 (a) SOI Drain current vs drain voltage in mA, (b) Drain current vs drain voltage in micro seconds

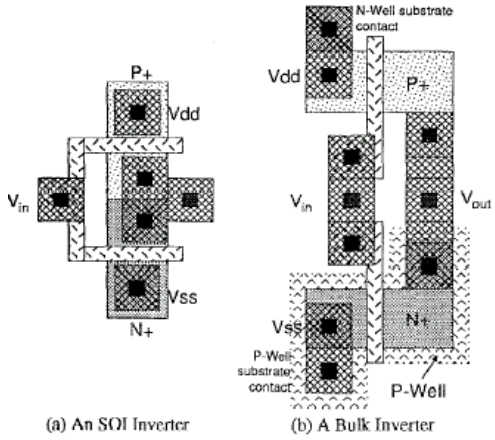

Figure 7 Inverter (a) An SOI Inverter, (b)A Bulk Inverter

6.1 THE PROCESS INTEGTATION OF SOI

Many techniques have been developed for producing a film of single-crystal silicon on top of insulator. Some of them are based on the epitaxial growth of silicon on either a silicon wafer covered with an insulator (homo-epitaxial techniques) or on a crystalline insulator (hetroepitaxial techniques). Other techniques are based on recrystallization of thin silicon layer from the melt (laser recrystallization, e-beam recrystallization and zone-melting recrystallization). Silicon-on-insulator can also be 2 produced from a bulk silicon wafer by isolating a thin silicon layer from the substrate through the formation and oxidation of porous silicon (FIPOS) or through the ion beam synthesis of a buried insulator layer(SIMOX, SIMNI and SIMON). Finally, SOI material can be obtained by thinning a silicon wafer boned to an insulator and mechanical substrate (wafer bonding BESOI). Every approach has its advantages and its pitfall, and the type of application to which the SOI materials is destined, dictates the material to be used in each particular case. SIMOX and UNIBOND are seems to be the ideal candidates for VLSI CMOS application, while wafer bonding is more adapted to bipolar and power applications.

Now we'll review some of the techniques have been used in producing the SOI materials.

A. HETRO-EPITAXIAL TECHNIQUES

Hetro-epitaxial Silicon-on-insulator films are obtained by epitaxially growing a silicon layer on a singlecrystal insulator (see figure 1). The films are grown using silane or dichlorosilane at temperatures around 1000C. All the insulating substrates have thermal coefficients which are 2-3 times higher than that of silicon which generated lot of stresses at interface. Therefore, thermal mismatch is the single most important factor determining the physical and electrical properties of silicon films grown on bulk insulators. Silicon-on-sapphire (SOS) is one of single most mature of all hetro-epitaxial materials used. SOS is fabricated by epitaxial growth of a Si film on Al2O3. The electrical properties may suffer from lateral stress, in-depth inhomogeneity of the film, and defective transition layer at the interface. Good quality 100 nm thick films, on 6 in. SOS wafers are now available.

B. HOMO-EPITAXIAL TECHNIQUES

Epitaxial lateral overgrowth, method consists of growing a singlecrystal Si film, from the substrate (i.e. the seed) through and above the SiO2 layer. ELO process requires a post-epitaxy thinning of the Si film, which can for example be achieved by using a patterned oxide, the silicon film in excess is removed leaving an isolated Si island (dotted line) in the BOX. The main application of ELO technique is the integration of 3-D stacked circuits. Coalescence of adjacent crystals, C) self-planarization of the surface.

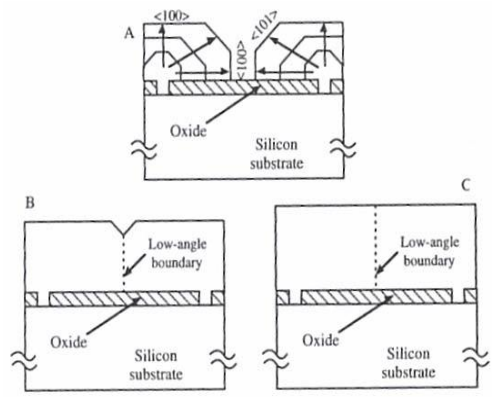

Fig-8: ELO technique. A) growth from seeding window, B) coalescence of adjacent crystals, C) self-planarization of the surface.

C. RECRYSTALLIZATION TECHNIQUES

MOS transistor can be fabricated on large grained polysilicon deposited on oxidized silicon substrate. But the presence of grain boundaries brings about low surface mobility and high thershould voltages.

Mobility and thershould voltages values can be improved by passivating the dandling silicon bond via hydrogen plasma treatment. High performance ICs however require much better device properties, and grain boundaries must be eliminated from the deposited silicon film. This is the goal of all recrystallization techniques such as Laser beam, E-Beam, zone melt recrystallization.

Laser and e-beam both are relatively slow processes (uses a pointed energy source) compared to zone melting method in which incoherent light or near IR source is used.

D. FIPOS: Full isolation by oxidized porous silicon

Anodic reaction is used to convert a particular region (predefined by p-type doping) of the Si wafer into porous silicon. During subsequent oxidation, the porous Si transforms very rapidly and selectively in a BOX. FIPOS may be able, in the future, to combine SOI circuits with electroluminescent porous Si devices.

E. SIMOX

In the last decade, the dominant SOI technology was SIMOX, which is synthesized by internal oxidation during the deep implantation of oxygen ions into a Si wafer. Annealing at high temperature restores the crystalline quality of the film. SIMOX 8 in. wafers have good thickness uniformity, low defect density (except threading dislocations: 104–106 cm-2), sharp Si–SiO2 interface, robust BOX, and high carrier mobility. Some basic processes of SIMOX are described in figure 9 and figure 10.

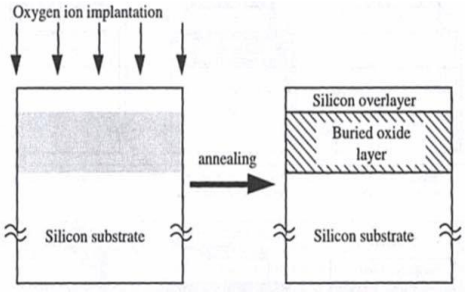

Fig-9: The principal of SIMOX: a heavy dose oxygen implantation into silicon followed by an annealing step produce a buried layer of silicon dioxide below thin single crystal silicon over layer.

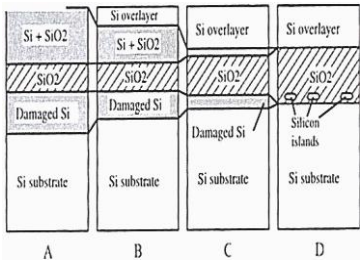

Fig-10: Evolution of the structure of the SIMOX structure as a function of post-annealing temperature (implant dose= 1.5 1018 cm-2, energy = 200 keV). A) as implanted, B)2-hr. annealing at 11500C , C) 6 hour annealing at 11850C, D) 6 Hr. annealing at 13000.

F. WAFER BONDING (WB)

Wafer bonding and etchback is another mature SOI technology. An oxidized Si wafer is mated to a second Si wafer.

When two flat, hydrophilic surfaces such as oxidized surfaces are placed against one another, bonding naturally occurs, even at room temperature, which forms the hydrogen bonds across the gap between two surfaces. After bonding, upper wafer is thinned down from

600microns to few microns to reach the target thickness of the silicon film. The thinning is usually done grinding followed by chemicalpolishing or grinding followed by etch-back process (preferred). In etch-back process a P+ layer is formed at the surface near the oxide where the etching is required and using proper etchant the bare Si surface above the bonded SiO2 is obtained with approximately 12nm surface tolerance.

G. UNIBOND

This material again belongs to the family of wafer bonding structures. But unlike the wafer bonding method, in UNIBOND, the etch back process is avoided. The revolutionary Smart-Cut mechanism uses the deep implantation of hydrogen (dotted line in figure 4) to generate microcavities. After bonding and annealing, the wafers separate naturally at a depth defined by the location of hydrogen microcavities which have eventually coalesced. The UNIBOND wafer is finished by touch polishing. The smart-cut approach has several outstanding advantages:

6.2 SOI FLOATING BODY

In a standard Bulk CMOS process technology, the P-type body of the NMOS Transistor is held at the ground voltage, while in

the Bulk CMOS process technology, a PMOS Transistor is fabricated in an N-well, with the transistor body held at the VDD supply voltage by means of a metal contact to the N-well.

In Silicon-On-Insulator process technology, the source, body and drain regions of transistors are insulated from the substrate. The body of each transistor is typically left unconnected and that results in a floating body. The floating body can get freely charged/discharged due to the transients (Switching) and this condition affects threshold voltage (Vt) and many other device characteristics.

The transistor area in SOI process is less because there is no need for metal contacts to Wells that are used for making MOS transistors.

6.3 FULLY DEPLETED SOI

In an NMOS transistor, applying a positive voltage to the gate depletes the body of P-type carriers and induces an N-type inversion channel on the surface of the body. If the insulated layer of silicon is made very thin, the layer fills the full depth of the body. A technology designed to operate this way is called a "fully depleted" SOI technology. The thin body avoids a floating voltage. In 45nm and below CMOS, the Vt can be tuned by a midgap metal gate leaving the fully-depleted body undoped. Higher channel mobility and hence higher performance are achieved, as well as lower variability from one device to another. Fully Depleted SOI enables a CMOS LP technology with un-doped body. It gives the best performance - low leakage couple, a perfect choice for Low Power Applications.

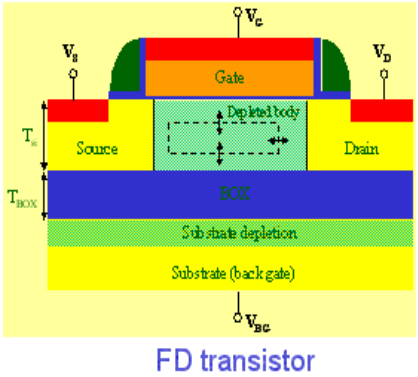

Figure 11 Fully Depleted SOI

6.4 PARTIALLY DEPLETED SOI

On the other hand, if the insulated layer of silicon is made thicker, the inversion region does not extend the full depth of the body. A technology designed to operate this way is called a "partially depleted" SOI technology. The undepleted portion of the body is not connected to anything. The exact voltage depends on the history of source, gate, and drain voltages leading up to the current time (the "history effect"). However, the voltage can be expected to fall within a known range.

The body voltage affects the conduction of the channel and therefore the switching speed and parasitic capacitance of the circuit. In an NMOS transistor, a lower initial body voltage results in a thinner inversion layer, lower conductivity, and slower switching. Conversely, a higher initial body voltage results in faster switching. In a PMOS transistor, the opposite is true; a lower initial

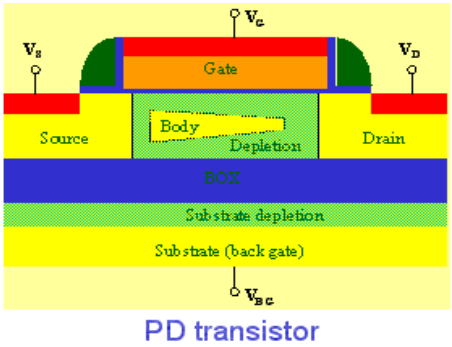

Figure 12 Partially Depleted SOI

6.5 LATCHUP ELIMINATION

Bulk CMOS relies on junction isolation between devices, while SOI uses dielectric isolation to surround the entire device sides and bottom. SOI has no wells into the substrate and therefore has no Latchup or leakage paths. It eliminates the need for guard rings, thus smaller area for same function.

6.6 BI-POLAR CURRENTS

There is a low gain parasitic bipolar transistor on every floating body SOI FET transistors. This bipolar transistor is in parallel with the FET transistor and could cause false switching to the off FET transistor. In general pass gate circuit has the highest bipolar current effect. It can be seen in fig 5

When both Source and Drain of Transistor are at High and Gate is at Low (in the case of a Pass Gate), the floating body will couple to high. When Source or Drain goes to Low then we will see a current pulse even when the gate is low. However over the years of the technology scaling, this bipolar current effect has been pretty much eliminated due to the reduction of the operating voltage of the 90nm node and beyond. In some extreme case, where the design has many transistors connected in parallel, the designer needs to verify the bipolar current to ensure the functionality of the circuit. This is particularly important if the design requires functional burn-in at a much higher voltage than the typical operating voltage condition.

6.7 SELF-HEATING

The insulation layer of the SOI wafer creates a potential temperature delta between devices called local (self) heating. Self-heating is evident at the high power regions. May not have huge impact on Digital circuits; however this effect must be considered for analogy type of circuits.

6.8 TEMPERATURE SENSITIVITY

SOI CMOS is much less sensitive to temperature than bulk. In all SOI processes, the leakage to the substrate is obviously suppressed. Furthermore in FD SOI, the Vt varies by about 2x less with temperature than in bulk.

6.9 BODY CONTACTS

In the digital circuits, the transistor operates as a switch and remains in a steady state most of the times. Modeling switching characteristics with Floating Body effects are slightly complicated, but it can be modeled. Where as in the Analog/Mixed/IO design modeling the behavior of linear characteristics circuit is very difficult with varying potential of the Floating Body as it changes the output impedance of the device and its Vt-matching to the next device. A Body Contact Transistor can be used as the current source or as any matching

transistors designs to eliminate the floating body effect in the SOI technology. However Body Contact has RC delay associated with it, and shows poor transient response due to high capacitance and resistance. Also Body Contacts do not scale with the Gate Length, and requires bigger Transistor size and Low density. Body contacts are used only where needed because they increase the layout area and decrease performance.

VII. CONCLUSION

The primary goal of this paper is to know the large scale integration and the techniques that involve in the integration. It also shows the brief description of the CMOS Bulk technology and SOI technology that are compared with each other. After studying the various circuit issues of both the technologies. SOI gives the superior results than Bulk technology, which increases the circuit performances, high reliability, removes the parasitic capacitance, punch through issue and the circuit compactness. Hence SOI technology is the leading and upcoming technology in both micro and nano electronics.

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