Design and Analysis of Level Shifter in High Voltage Transmitter

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Abstract: A high voltage transmitter integrated circuit for ultrasound medical imaging is implemented using 90nm technology.The high voltage transmitter consists of level shifter and output drivers to increase the voltage, with reduced delay,that drives the capacitive micro-machined ultrasound transducer to produce acoustic signal in medical applications .The performance of various level shifters are compared. The level shifter generates 20V pulses from the input of 10V. The level shifter is designed using 90nm technology in HSPICE.

***Key words*:** CMUT, Level shifter, CMOS.

I. INTRODUCTION

Ultra sonic imaging is an important modality for medical diagnosis. Compared with other imaging modalities , ultrasound is relatively low cost and harmless to human health and has decent resolution. Modern ultrasonic imaging systems are becoming increasingly complex and powerful, yet compact. The trend toward highly integrated ultrasonic imaging solutions to enable portable or even wearable ultrasound applications in hospital and at home. capacitive micro machined ultrasonic transducers recently emerged for better system integration cmut technology offers advantages such as improved bandwidth, ease of fabricating large arrays, and potential for integration with electronics.For the transmitter , high-voltage linear amplifiers are commonly used to drive the PZT loads to achieve a linearity and acceptable efficiency. In case of CMUT load, linear amplifiers are not optimum and degrades the overall power efficiency of the power efficiency of the transmitter stage. High voltage pulser can be used instead of amplifiers so that the power dissipated while charging and discharging capacitance does not contribute to the acoustic output. The transmitter efficiency is defined as the ratio between the useful acoustic power and the total power dissipated. One of the main issues is the area-hungry HV transmitter in the interfacing analog front-end IC.The HV transmitter usually utilizes large-size HV double-diffused MOS (DMOS) transistors to generate HV output pulse signals to drive the CMUT to produce large acoustic pressure while maintaining the reliability to prevent possible device junction breakdown. In this brief, a highly integrated HV transmitter utilizing standard CMOS transistors targeted for ultrasound medical imaging in a highly integrated needle device for obstetrics and gynecology applications is presented[2]. In this alternate implementation highly-integrated, high-voltage pulsers quickly switch the transducer element to the appropriate programmable high-voltage supplies to generate the transmit waveform. To generate a simple bipolar transmit waveform, a transmit pulser alternately connects the element to a positive and negative transmit supply voltage controlled by the digital beamformer. More complex realizations allow connections to multiple supplies and ground in order to generate more complex multilevel waveforms with better characteristics.The slew rate and symmetry requirements for high-voltage pulsers have increased in recent years due to the popularity of second-harmonic imaging. Second-harmonic imaging takes advantage of the nonlinear acoustic properties of the human body. These nonlinearities tend to translate acoustic energy at fo to energy at 2fo. Reception of these second-harmonic signals has, for a variety of reasons, produced better image quality and is now widely used.A high-voltage (HV) transmitter integrated circuit for ultrasound medical imaging applications was implemented using 0.18-μm CMOS technology. The HV transmitter achieves high integration by only employing standard CMOS transistors in a stacked configuration with dynamic gate biasing circuit while successfully driving the capacitive micro machined ultrasound transducer device immersed in an oil environment without breakdown reliability issues. The HV transmitter including the output driver and the voltage level shifters generates over 10-Vp−p pulses at 1.25-MHz frequency.

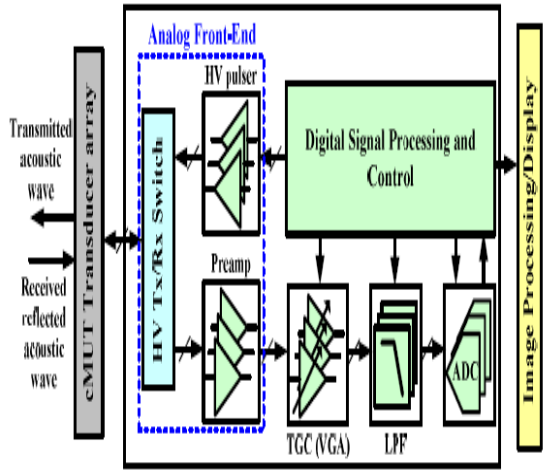

Fig1.Block diagram of ultrasound medical system

A fully integrated high-voltage (HV) front-end transducer for ultrasonic sensing applications. This includes a programmable HV dc–dc converter (HVDC), a drive amplifier, and a tuneable pulse generator. The HVDC is based on a multistage two-phase voltage doubler and static level up shifters. The drive amplifier is composed of a static level-up stage and a Class-D switching output stage.In this paper,a static level-up shifter(LUS) is used in each stage as a clock generator, in order to increase the voltage exponentially. By cascading voltage-doublers,the output voltage obtained.

Each stage consists of a voltage doubler circuit, a charge transfer circuit, a static LUS and a static level-up stage . The voltage doubler circuit is composed of cross-connected HVnMOS transistors and pumping capacitors. The charge transfer circuit is composed of a pair of HVpMOS transistors .

II. LITERATURE SURVEY

CMUT fabrication can be done using several processes such as wafer bonding,simple wafer bonding,LOCOS process,thick-buried oxide process,sacrificial release process and piston CMUT structure and process. These can be integrated with front end electronics to provide high voltage according to their applications. Transmitter pulsers and receive amplifiers are used. The advantages of integrating front end electronics with CMUT :Better utilization of large arrays and Improves receive sensitivity.Ultrasound is widely used as a diagnostic imaging modality in many clinical applications and has recently received increased attention and acceptance as a therapeutic tool.

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With scaling of Vt sub-threshold leakage power is increasing and expected to become significant part of total power consumption.In present work three new configurations of level shifters for low power application in 0.35µm technology have been presented. The proposed circuits utilize the merits of stacking technique with smaller leakage current and reduction in leakage power. Conventional level shifter has been improved by addition of three NMOS transistors, which shows total power consumption as compared to with existing circuit. Single supply level shifter has been modified with addition of two NMOS transistors that gives total power consumption.Contention mitigated level shifter (CMLS) with three additional transistors [3]shows total power consumption of 396.75pW. Three proposed circuit's shows better performance in terms of power consumption with a little conciliation in delay.Output level of 3.3V has been obtained with input pulse of 1.6V.Level Shifters are required between core circuits and I/O circuits interface where low voltage logic signals from chip core are shifted to high voltage level at which pad Ring is working. Since the level shifter circuit consumes power and has a considerable delay, how to optimize the performance to gain low power and small delay and how to minimize the number of level shifters are important in the voltage scaling technique.In paper[4], different types of level shifter are focused.Driven by the need to reduce power consumption and maintain high reliability in leading edge integrated circuits, the nominal operating supply voltage for these devices is falling steadily.

A voltage level conversion at the input of a particular voltage domain will require all the supply voltages of signals coming to this voltage domain from other voltage domains whose voltage level is lower than its own voltage level. This may result in routing congestion, excessive area utilization and also

may pose restrictions on module placement. The routing of additional supply voltages can be avoided by sending a signal (which is going to a different voltage domain) in both polarities . However, this strategy would require one additional wire per signal and hence could lead to routing congestion. This problem is further aggravated by the increasing number of voltage domains in SoCs and multi-core architectures. Additional complexity is encountered if the voltage domains have variable voltages[5], which requires a domain to receive the supply voltages of every other domain.

III. BASIC LEVEL SHIFTER

3.1 OVERVIEW OF LEVEL SHIFTER

The level shifter is used to convert high voltage levels to low voltage level or vice-versa.Bi-directional level shifters and translator circuits are used to interface between applications with different supply voltage and input-output voltage levels.Level shifter are the bridges that transform from low core voltage to high voltage.There are different types of level shifter such as single supply level shifter and dual supply level shifter.The single supply level shifter allows communication between modules without adding any extra supply pin,it have advantages over dual supply level shifter in terms of pin count,congestion in routing and overall cost of the system.

3.2 BASIC OPERATION OF LEVEL SHIFTER

The schematic of level shifter is shown below. Conventional level shifter using 10 transistor with low voltage supply VddL and high voltage supply VddH. The conventional level shifters have disadvantages of delay variation due to different current driving capabilities of transistors, large power consumption and failure at low supply core voltage VddL

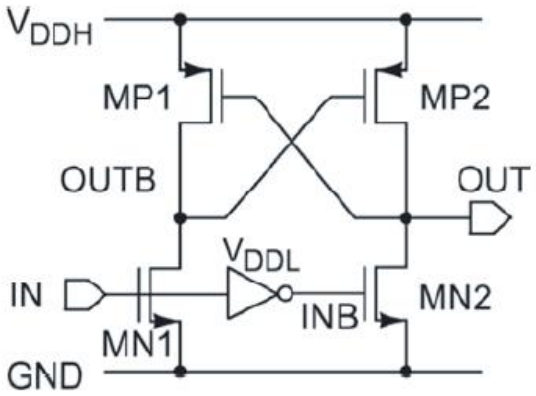


Fig 2.Block diagram of level shifter

3.3 SINGLE SUPPLY LEVEL SHIFTER

The needs for two voltage supply limit the physical placement of such level shifter to the boundary of high and low voltage designs which restricts the physical design flexibility. To address this, a novel level shifter which requires only one supply VDDH to convert the low Voltage signal to the higher voltage has been proposed. It makes the placement much more flexible in the entire high voltage regions. The threshold drop (Vtn) across the NMOS MN1 provides a virtual VDDL to the input inverter (MP2, MN2). The output stage is a half latch which pulls up the input of the inverter (MP3, MN3) to VDDH in order to avoid leakage. When input signal (IN) is HIGH, the voltage at node T1 is (VDDH-Vtn) with the purpose of reducing gate to source voltage of MP2 to turn it OFF. When the input signal (IN) is LOW, the feedback transistor MP4 turns ON so that charges node T1 to VDDH to compensate the threshold drop. Hence the supply voltage of inverter (MP2-MN2) is dynamically switched between VDDH-Vtn and VDDH depending upon the input state.

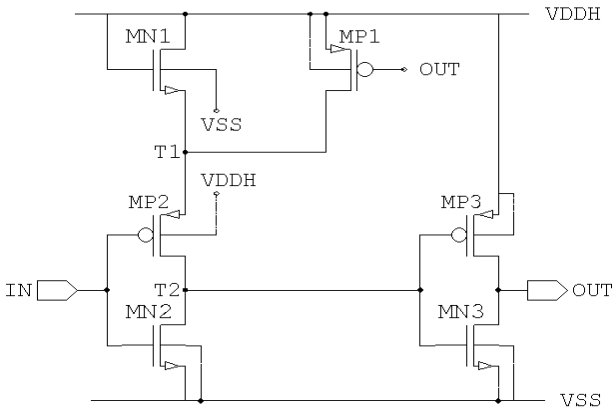


Fig.3 Schematic of single supply level shifter

3.4 EXISTING LEVEL SHIFTER

A high-voltage (HV) transmitter integrated circuit for ultrasound medical imaging applications was implemented using 180nm CMOS technology. The HV transmitter achieves high integration by only employing standard CMOS transistors in a stacked configuration with dynamic gate biasing circuit while successfully driving the capacitive micro machined ultrasound transducer device. The HV transmitter including the output driver and the voltage level shifters generates over 10-Vp−p pulses

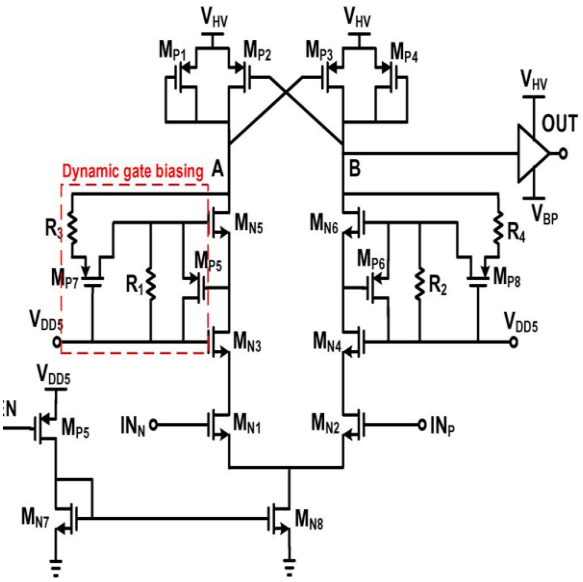


Fig.4 Schematic of Existing level shifter in HV transmitter

3.5 MODIFIED LEVEL SHIFTER

The level shifters can be designed to convert low voltage (5V) to high voltage (20V).We propose a low-power single- input level shifter as shown in Fig.5. To reduce power consumption, there is no diode-connected TFT in the circuit and the pull-up TFTs and the pull-down TFTs are never turned on simultaneously. In addition, only a single input signal is required by this circuit,which simplifies the interface design considerably.This design minimizes the leakage .Reliability is high compared to existing method. Delay can be reduced by using HSPICE tool(90nm)

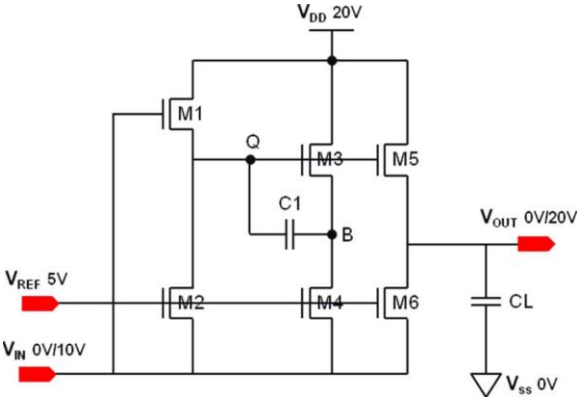
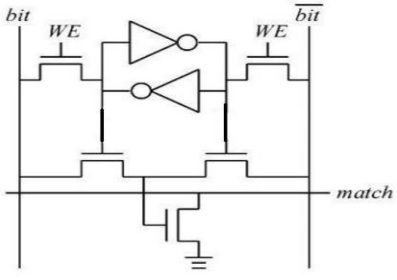


Fig.5 Modified Single Supply Level Shifter

4 SIMULATION RESULTS



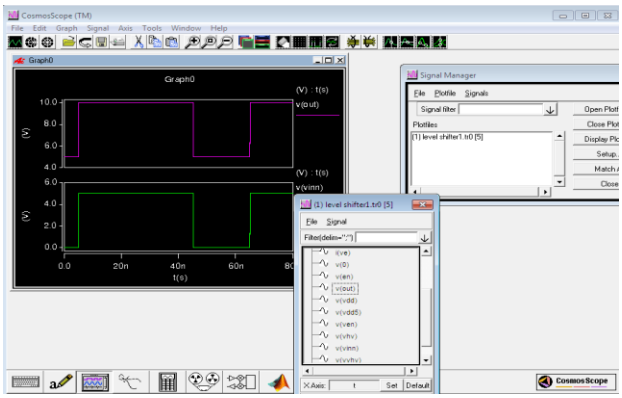


Fig.6 Waveform of existing level shifter

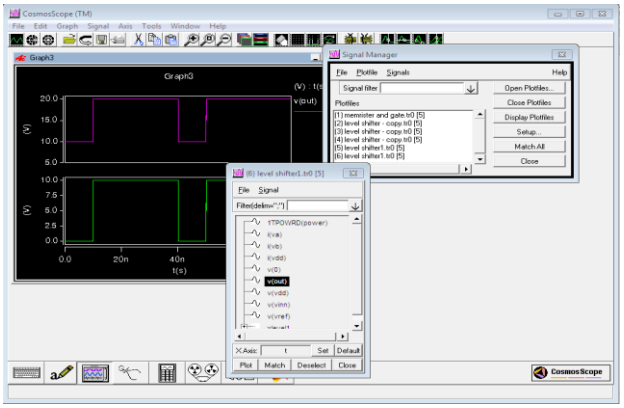


Fig.7 Waveform of modified level shifter

5. CONCLUSION

A new level shifter have been designed in this paper. The various design of level shifter and proposed design is simulated with a 90nm CMOS technology. Further the voltage is increased with reduced delay of the existing circuit. Therefore the proposed design can be used in ultrasound medical applications.

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