Performance evaluation of the CMOS Full adders in TDK 90 nm Technology

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Abstract- This paper presents power analysis of the full adder cells reported as having a low PDP (Power Delay Product), by means of speed, power consumption and area. These full adders were designed upon various logic styles to derive the sum and carry outputs. Two new high-speed and low-power full adder cells designed with an alternative internal logic structure and pass-transistor logic styles that lead to have a reduced PDP (Power-delay product). These all full adder cells designed using a TDK 90 nm CMOS technology.

Keywords- Adder circuits, pass transistor logic, power delay product, layout design.

I. Introduction

In portable electronic devices, it is important to prolong the battery life as much as possible. Adder is the core component of an arithmetic unit. The efficiency of the adder determines the efficiency of the arithmetic unit. Various structures have evolved trying to improve the performance of the adder in terms of area, power and speed. Low power design with high speed of operation is more essential.

The fundamental arithmetic operation is Addition and it is used extensively in many VLSI systems such as application-specific DSP architectures and microprocessors. in addition to its main task, which is adding two binary numbers, it is the nucleus of many other useful operations such as subtraction, multiplication, division, address calculation, etc. in most of these systems the adder is part of the critical path that determines the overall performance of the system.

The amount of energy spent during the realization of a determined task relates to PDP and stands as the more fair performance metric when comparing optimizations of a module designed and tested using different technologies, operating frequencies. The PDP exhibited by the full-adder would affect the system's overall performance.

The new full adder cell designed using an alternative logic structure that is based on the multiplexing of the Boolean functions XOR/XNOR and AND/OR, to obtain the SUM and CARRY outputs, respectively. These full adders show to be more efficient on regards of power consumption and PDP when compared with other ones reported previously as good candidates to build low-power arithmetic modules. And all these full adders designed using TDK 90 nm Technology and simulated using mentor graphics EDA tool with BSIMv3 (model 49). And the layouts of all these full adders designed in Icstation of Mentor Graphics.

II. Standard Full Adders Designs

Transmission function theory was used to build a full adder formed by three main logic blocks: a XOR-XNOR gate to obtain A ⊕ B and A ⊙ B signals (Block 1), and XOR blocks or multiplexers to obtain the SUM (So) and CARRY (Co) outputs (Blocks 2 and 3), as shown in Figure 1.

This logic structure is based on the full adder's true-table shown in Table I, and it has been adopted as the standard internal configuration in most of the enhancements developed for the 1-bit full adder cell. After a deep comparative study, the most efficient realization for block I was extracted: the one implemented with SR-CPL logic style. But another important conclusion has pointed out over there: the major problem on regards of propagation delay for a full adder built upon the logic structure shown in Figure 1 is that it is necessary to obtain the A ⊕ B and A ⊙ B intermediate signals, which are then used to drive other blocks in order to generate the final outputs. Thus, the overall propagation delay and, in most of the cases, the power consumption of the full adder, depend on the delay and voltage swing of the A ⊕ B and A ⊙ B signals, generated within the cell.

Therefore, to increase the operational speed of the full adder, it is necessary to look out for a new logic structure that avoids the generation of intermediate signals used to control the selection or transmission of other signals located on the critical path.

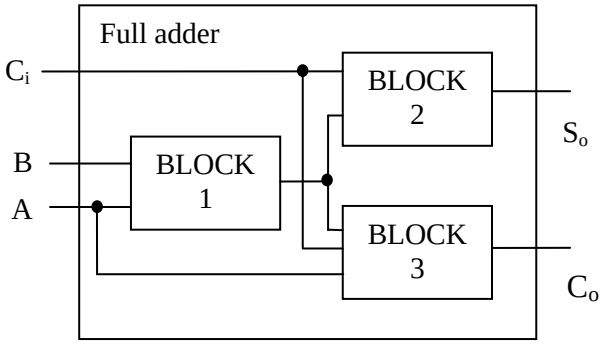

Fig.1. Full-adder cell formed by three main logical blocks.

III. Alternative Logic Structure For A Full Adder

Examining the full-adder's true-table in Table I, it can be seen that the *So* output is equal to the A ⊕ B value when C=0, and it is equal to A ⊙ B when C=1. Thus, a multiplexer can be used to obtain the respective value taking the C input as the selection signal. Following the same criteria, the *Co* output is equal to the A · B value when C = 0, and it is equal to A + B value when C = 1.

TABLE I
True-Table For A 1-Bit Full-Adder: A, B, And C Are Inputs; So And Co Are Outputs

C	B	A	So	Co
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Again, C can be used to select the respective value for the required condition, driving a multiplexer. Hence, an alternative logic scheme to design a full-adder cell can be formed by a logic block to obtain the A ⊕ B and A ⊙ B signals, another block to obtain the A · B and A + B signals, and two multiplexers being driven by the C input to generate the *So* and *Co* outputs, as shown in Fig. 1 .

The features and advantages of this logic structure are as follows.

• There are not signals generated internally that control the selection of the output multiplexers. Instead, the C input signal, exhibiting a full voltage swing and no extra delay, is used to drive the multiplexers, reducing so the overall propagation delays.

• The capacitive load for the C input has been reduced, as it is connected only to some transistor gates and no longer to some drain or source terminals, where the diffusion capacitance is becoming very large for sub-micrometer technologies. Thus, the overall delay for larger modules where the C signal falls on the critical path can be reduced.

• The propagation delay for the *So* and *Co* outputs can be tuned up individually by adjusting the XOR/XNOR and the AND/OR gates; this feature is advantageous for applications where the skew between arriving signals is critical for a proper operation (e.g., wave pipelining), and for having well balanced propagation delays at the outputs to reduce the chance of glitches in cascaded applications.

• The inclusion of buffers at the full-adder outputs can be implemented by interchanging the XOR/XNOR signals, and the AND/OR gates to NAND/NOR gates at the input of the multiplexers, improving in this way the performance for load-sensitive applications.

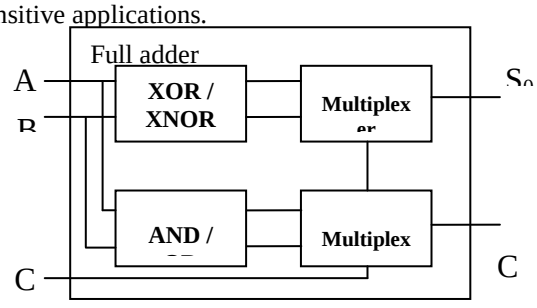

Fig. 2. Alternative logic scheme for designing full-adder cells.

Two new full-adders have been designed using the logic styles DPL and SR-CPL, and the new logic structure presented in Fig. 3. Fig. 4 presents a full-adder designed using a DPL logic style to build the XOR/XNOR gates, and a pass-transistor based multiplexer to obtain the *So* output. In Fig. 4, the SR-CPL logic style was used to build these XOR/XNOR gates. In both cases, the AND/OR gates have been built using a powerless and groundless pass-transistor configuration, respectively, and a pass-transistor based multiplexer to get the *Co* output.

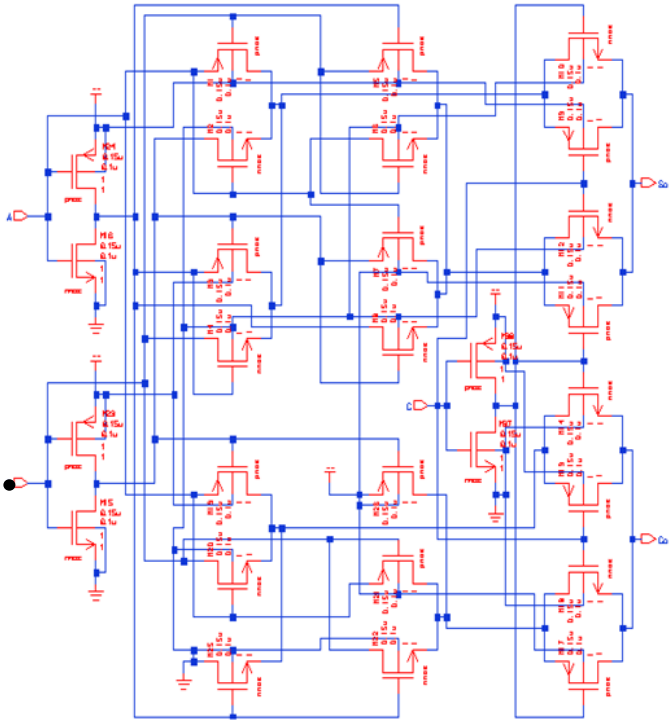

Fig. 3. Full-adder designed with a DPL logic style.

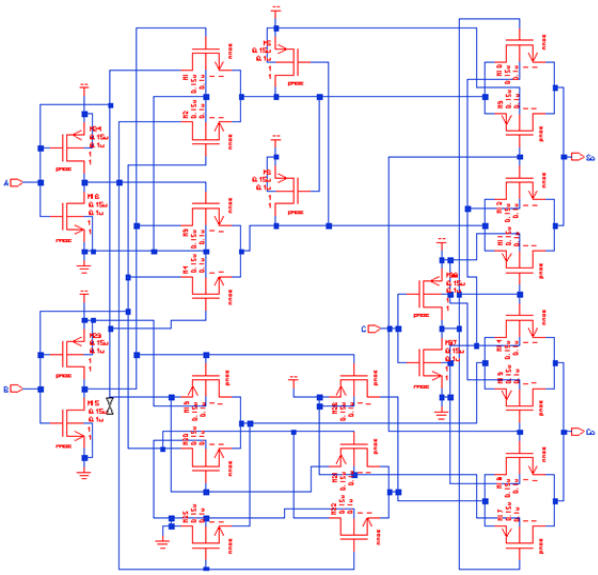

Fig 4. Full-adder designed with the SR-CPL logic style.

IV. Simulation Setup

The test bed used to simulate the full adders being compared is shown in Figure 5. This simulation environment has been commonly used to compare the performance of the full adders.

The advantage of using this test bed is that the Following power components are taken into account, besides the dynamic one:
The short-circuit dissipation of the inverters connected at the full adder inputs.

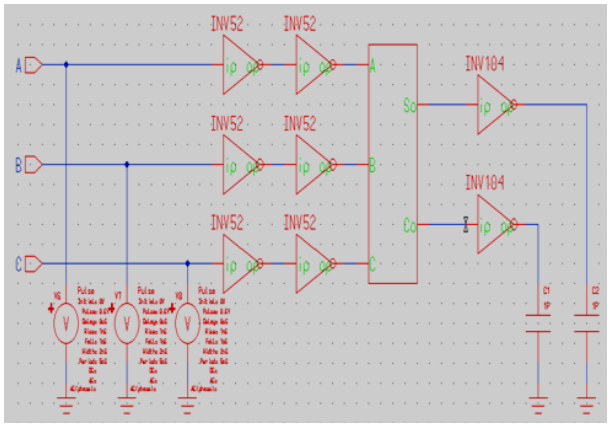

Fig 5. Test bed used for simulating the full-adders under comparison.

This power consumption varies according to the capacitive load that the adder module offers at the inputs. Even more, the energy required to charge and discharge the full adder internal nodes when the module has no direct power supply connections (such is the case of pass-transistor logic styles), comes through these inverters connected at the full adder inputs.

- The short-circuit consumption of the full adder itself, as it is receiving signals with finite slopes coming from the buffers connected at the inputs, instead of ideal ones coming from voltage sources.
- The short-circuit and static dissipation of the inverters connected to the outputs of the full adder due to the finite slopes and degraded voltage swing of the full adder output signals.

The importance of including the effects and power consumption of the buffers connected at the inputs and outputs of the full adder cell come from the fact that the module is always going to be used in combination with other modules to build a larger system, and these static inverters are a good generalization for any other module to be considered.

V. Simulation Results

Seven full adders were compared on regards of power consumption and delay. They were named: new14T[1], HPSC[2], HYBRID[3], HYBRID CMOS[4], CPL[5], DPL and SR-CPL[6].

The schematics and layouts were designed using a TDK 90 nm CMOS technology, and simulated using the BSIM3v3 model (level 49) and the post-layout extracted netlists containing R and C parasitics. Simulations were carried out using ICSTUDIO in Mentor Graphics Eda Tool. Table 2 shows the simulation results for full-adders performance comparison, regarding power consumption, propagation delay, PDP and area.

The ICSTUDIO in Mentor Graphics EDA Tool simulations showed that of 59.56% power savings and 57.51% for the PDP for the joint optimization at 5v. And 52.32% power savings and 48.83% for the PDP for the joint optimization at 1.8v.

TABLE III
Simulation Results of the Full-Adders Compared

S. No.	Name of the full adder	No. of transistors	Frequency	Area (µm2)		
				L	W	L*W
1	NEW14T	14	200 MHZ	5.14	7.75	39.83
2	HYBRID CMOS	24	200 MHZ	4.92	9.07	44.61
3	HPSC	22	200 MHZ	6.49	7.60	49.31
4	HYBRID	26	200 MHZ	5.76	9.57	55.11
5	CPL	28	200 MHZ	7.37	8.29	61.10
6	DPL	28	200 MHZ	4.89	7.95	38.87
7	SRCPL	26	200 MHZ	5.40	7.72	41.69

S. No.	Name of the full adder	at 5v Supply voltage				
		Power dissipation(uW)	Propagation delay (ps)			PDP (uw*ps)
			Sum	Carry	Average delay	
1	HYBRID	1206.5	147.1	160.59	153.8	185668.28
2	HPSC	1214.6	146.6	152.19	149.3	181455.16
3	HYBRID CMOS	912.2	205.4	171.19	188.3	171815.14
4	NEW14T	983.8	152.3	146.70	149.5	147081.88
5	CPL	540.3	205.7	204.79	205.2	110931.59
6	DPL	491.3	189.1	176.56	182.8	89837.66
7	SRCPL	490.9	139.9	181.49	160.6	78893.24

S. No.	Name of the full adder	at 1.8v Supply voltage				
		Power dissipation (uW)	Propagation delay (ps)			PDP (uw*ps)
			Sum	Carry	Average delay	
1	NEW14T	8.85	136.1	115.4	125.8	1113.33
2	HYBRID CMOS	6.13	153.9	131.8	142.9	876.65
3	HYBRID	6.57	108.3	133.3	120.8	793.54
4	HPSC	6.57	108.2	125.0	116.6	765.83
5	CPL	4.65	142.6	147.1	144.8	673.27
6	DPL	4.23	133.6	158.8	146.2	617.93
7	SRCPL	4.21	98.8	148.7	123.6	521.23

VI. Conclusions

The design of high-speed low-power full adder cells based upon an alternative logic approach has been presented. MENTOR GRAPHICS EDA TOOL simulations have shown a great improvement on regards of power-delay metric for the proposed adders, when compared with previously published realizations designed with TDK 90 nm technology.

The full adders designed upon this logic structure and DPL and SR-CPL logic styles, exhibit a delay around 134.9 ps and power consumption around 4.22 µW at 1.8v and the delay is around 171.7 and power dissipation is 491.1 µW at 5v supply voltage, for an overall reduction of 81% respect to the best featured one of the other adders been compared, but in general about 50% respect to the other ones.

Some work can be done in the future on the design of 45 nm technology of high-speed low-power full adders.

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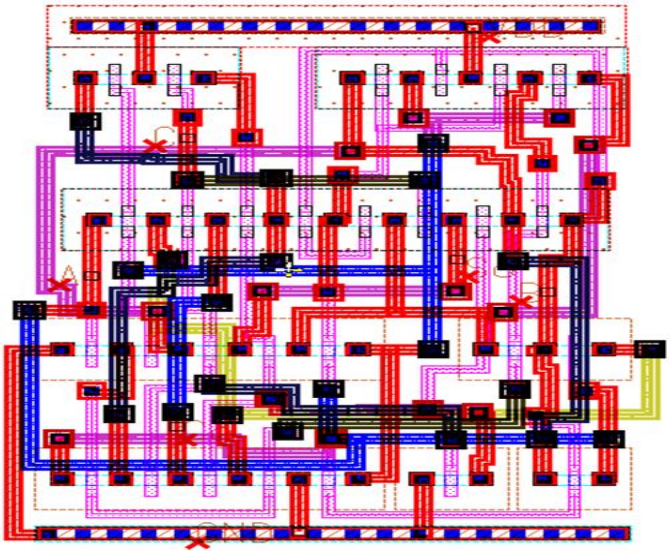

Fig. 6. Layout of the DPL full-adder.

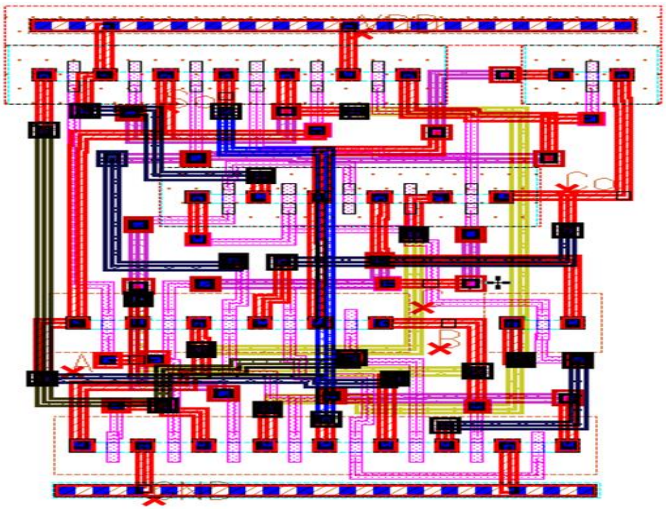

Fig. 7. Layout of the SRCPL full-adder.

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